Equalization and Near-End Crosstalk (NEXT) Noise Cancellation for 20-Gbit/sec 4-PAM Backplane Serial I/O Interconnections

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Equalization and Near-End Crosstalk (NEXT) Noise Cancellation for 20-Gbit/sec 4-PAM Backplane Serial I/O Interconnections

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SUMMARY

In this dissertation, the combined solution of the Feed-Forward Equalizer (FFE) and Near-End Crosstalk (NEXT) noise cancellation technique was developed to increase data throughput and to improve link quality in 20-in FR4 legacy backplane application. Backplane channel characteristics such as loss and coupling noise were measured and characterized to develop the corresponding behavioral channel model. Based on this channel model, the system architectures of the FFE and NEXT noise canceller were suggested and the corresponding building block requirements were defined.

The receiver-side FFE with 4-tap Finite Impulse Response (FIR) filter structure was adopted as the optimum equalizer topology for the backplane channel considered herein. The 4-tap FIR filter consists of tap delay line with tap-spacing 33 ps and bi-polar linear tap-gain amplifiers. The tap coefficients were calculated with Minimum-Mean-Squared-Error (MMSE) algorithm to minimize the overall noise effect of thermal and coupling noise components. A 4-tap FIR filter IC was designed and fabricated with a 0.18-um CMOS process technology. The experiment results showed 20-Gbit/sec 4-PAM signal and 10-Gbit/sec NRZ signal were successfully equalized for 20-in FR4 legacy backplane channel. Moreover, the suggested NEXT noise cancellation technique consists of coarse- and fine-cancellation stages. The corresponding building block ICs such as 7-tap FIR filter, tunable active Pole-Zero (PZ) filter, and a temporal alignment delay line were fabricated with the 0.18-um CMOS process technology. The experiment results showed that 6-dB Signal-to-Noise Ratio (SNR) improvement was achieved by the developed NEXT noise cancellation technique.

CHAPTER I

INTRODUCTION

With the emergence of the internet, network data traffic has been increased explosively. Moreover, computers have evolved from simple calculators to high-definition multi-media players. As a result, the system upgrade of the networking equipment has been immense challenge to meet ever increasing demand of broadband network capacity. Advances in optical links and supporting electronics have dramatically increased the speed and amount of data traffic handled by a network system

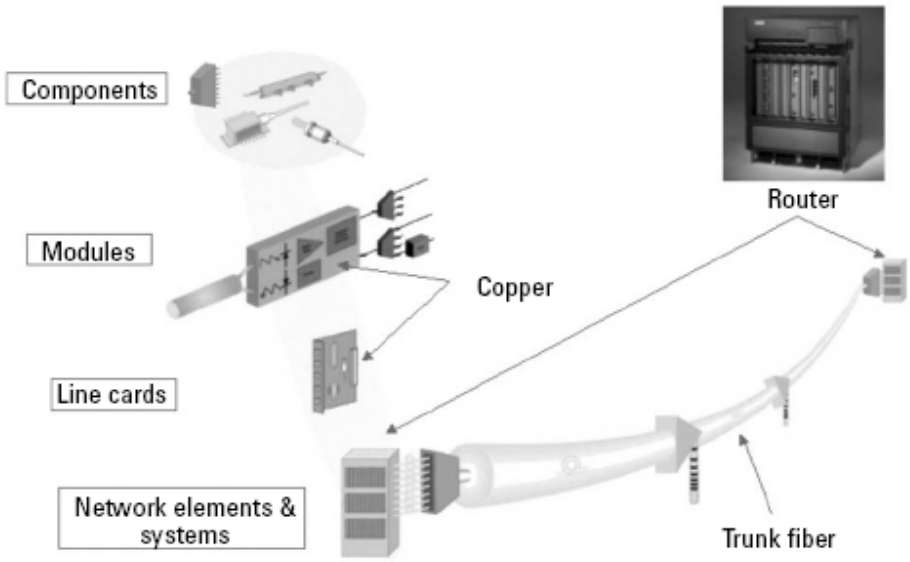


Figure 1.1. High-speed network system configuration

Figure 1.1 shows the high-speed networking system configuration. High-speed optical transceiver modules and networking processors are mounted on a line card. Several line

cards are plugged into the backplane of the network router system. In most high-speed networking applications, sophisticated Input/Output (I/O) interfaces are used to transfer multi-Gbit/sec data streams between the control processors on each line card. This physical layer copper interface creates new problems in signal integrity performance. One of the most challenging areas for realizing high-speed networking system is backplane. Backplanes, shown in Figure 1.2, comprise the physical highway and infrastructure for this data transmission and are often entrenched and difficult to change without great effort or trouble. As a result, legacy backplanes are not keeping pace with other technical improvements for delivery of multi-gigabit serial data traffic and are becoming a critical bottleneck.

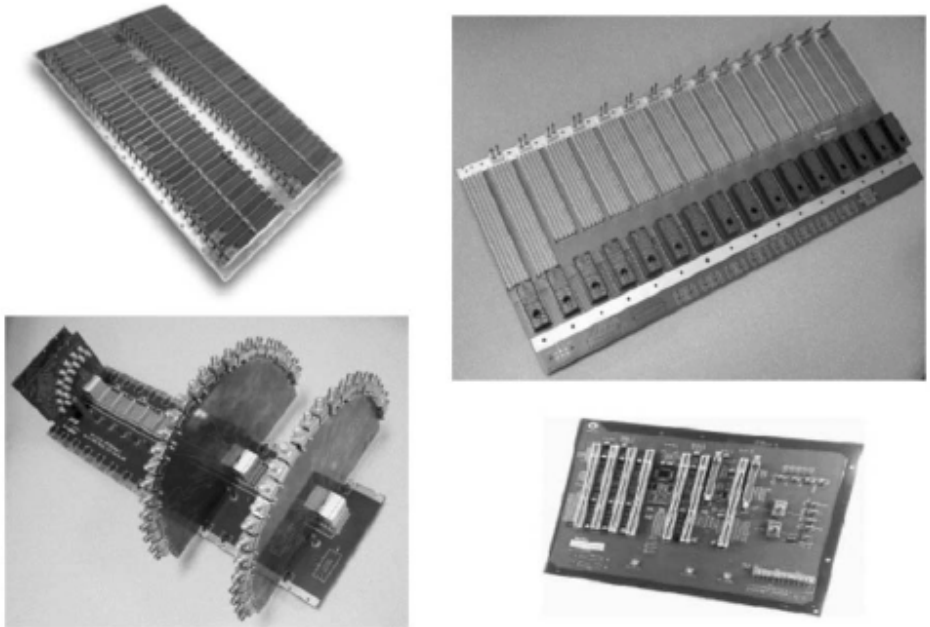


Figure 1.2. Pictures of typical legacy backplanes

The primary physical impediments to high data rates in legacy backplane channels are the frequency dependent loss characteristics of copper channels and the interference from adjacent channels. These effects become more severe as the data rate increases beyond 2 Gbit/sec. Above rates of 5 Gbit/sec, the skin effect and dielectric loss in backplane copper channels distort the signal to such a degree that signal integrity is severely impaired [1-4]. This dispersive forward channel characteristic contributes to the Inter-Symbol Interference (ISI).

As the bandwidth of the signal increases, unshielded pins in connectors radiate spurious signals. When these pins are in close proximity, adjacent "aggressor" channels can couple unwanted signals to contribute to noise in the "victim" channel. This noise is characterized as crosstalk noise and can occur at a connector close to the receiver in the channel, Near-End Crosstalk (NEXT) or at a connector farther down the channel, Far-End Crosstalk (FEXT). Because the coupled noise increases with frequency, this coupling noise becomes the main impairment factor preventing one from achieving desired bit error rate and jitter performance above 5 Gbit/sec [3-5].

The channel bandwidth limitation can be addressed by using dielectric materials with better loss characteristics, compensation of the channel induced loss via equalization techniques at the transmit and/or receiver side, and using more spectrally efficient signaling schemes [1-3], [6-7]. Digital equalization techniques have traditionally been used to reduce ISI in band-limited wire line applications. However, such techniques require high resolution Analog-to-Digital Converters (ADCs) with sampling rates at or above the symbol rate. The increased circuit complexity and power consumption required to apply these techniques to high-speed serial data transmission are prohibitive

at the considered data rates. Hence, analog or mixed-signal equalization techniques are attractive alternatives for multi-Gbit/sec serial transmission [1, 2]. In [1], a pre-emphasis transmitter was implemented for 10-Gbit/sec 4-level pulse amplitude modulation (4-PAM) transmission over coaxial cable. This pre-emphasis equalization technique causes the enhancement of coupling effect in the backplane channel. Thus, receiver side equalization technique is considered suitable to backplane signaling environment. *Wu et al.* [8] introduced an analog equalizer employing a Finite Impulse Response (FIR) filter for 10-Gbit/sec binary data transmission over multi-mode fiber. A passive LC-ladder structure was adopted as a delay line in FIR filter implementation. Due to intrinsic loss problem of passive delay line approaches, this analog equalizer has the problem of the limited number of taps in the FIR structure. Therefore, development of a novel delay line structure is still requested.

To alleviate NEXT noise contributions, sophisticated connectors and active noise cancellation techniques have been proposed [9-11]. Techniques that involve drastic physical changes to the backplane environment like replacing dielectrics and connectors with improved products are difficult to implement without an invasive overhaul of the system. This leaves equalization of the lossy channels, active cancellation of the NEXT noise, and the use of spectral efficient signaling schemes as the most efficient means to achieve high data rates.

The combination of techniques is critical as data rate increases. The dispersive forward channel characteristics can be alleviated by equalization techniques that boost the high frequency components of the signals [1-4]. However, because the NEXT noise channel characteristics resemble a high-pass filter, applying equalization to recover the

transmitted signal in the presence of NEXT noise will result in boosting the high frequency components of both the received signal and NEXT noise, canceling any benefits from equalization. To realize rates at 10 Gbit/sec and above, it becomes imperative that crosstalk noise be cancelled before equalization is applied. An integrated solution also allows for adaptability to compensate for changes in the channel due to variations in different vendor products, differences in channel length, and environmental effects.

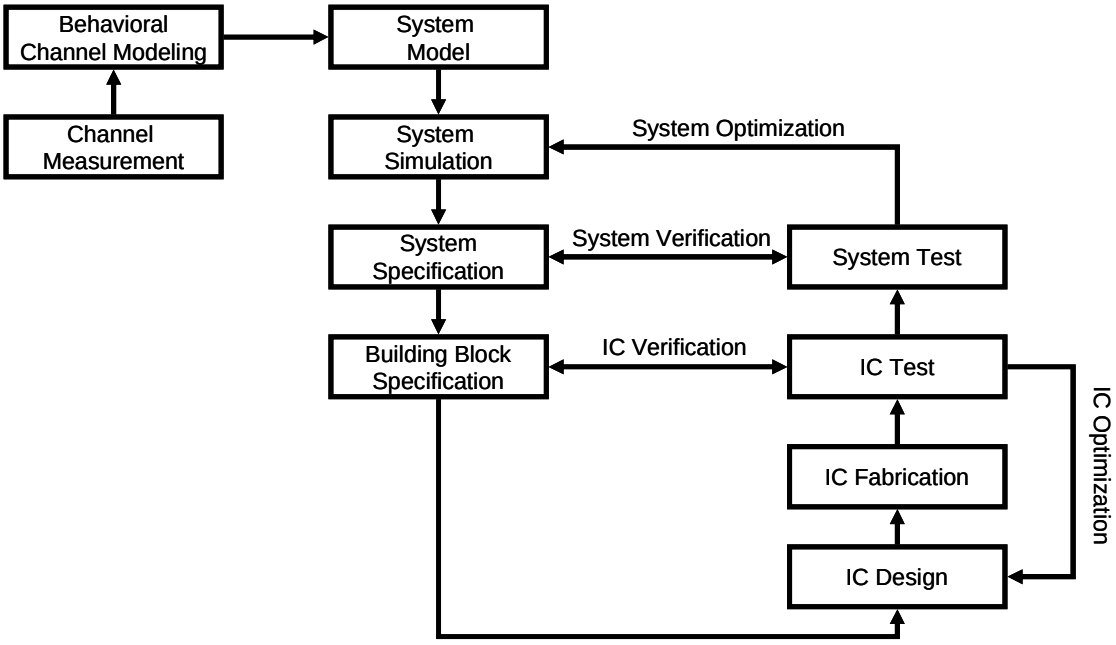


Figure 1.3. The systematic approach adopted in this work to mitigate the channel effects.

In this dissertation, the signal integrity problems in legacy backplane signaling environment and the corresponding solutions are investigated through a series of procedures, as shown in Figure 1.3. Legacy backplane channels are measured and characterized to develop behavioral channel model. Based on this channel model, the impacts of the channel's problems on the signal integrity are evaluated and the

corresponding solutions are investigated. System architectures are built and signal processing techniques are applied to mitigate the channel's effects. Each function of the signal processing technique is matched to the IC building block. From this thorough system simulation, the optimum system control conditions and the circuit specifications can be well defined. Based on these specifications, the building block integrated circuits (ICs) are designed and fabricated. The fundamental functions of the fabricated ICs are tested to verify their functionality and compared to their target specifications resulting from system simulations. Then, system functionality is tested to show the performance of channel effect mitigation predicted in the system simulation. Using these test results, the system simulation is repeated to reflect the practical implementation issues such as noise and bandwidth limitation of the adopted fabrication process technology. Correspondingly, the IC designs are optimized to meet the functional requirement obtained in the system simulation.

In this dissertation, a receiver side integrated complementary metal oxide semiconductor (CMOS) solution for extending data rates into the tens of Gbit/sec on legacy FR-4 backplanes is presented. 4-level Pulse Amplitude Modulation (4-PAM) signaling scheme is suggested with the combination of a Feed-Forward Equalizer (FFE) and a NEXT noise canceller to achieve 20-Gbit/sec transmission over backplane channels. The building block circuits are implemented with 0.18um-CMOS process technology.

The original contribution of this dissertation includes:

1. First 0.18-um CMOS FFE for 20-Gbit/sec throughput over 20-in FR4 legacy backplane channel.

2. First 0.18-um CMOS NEXT noise canceller adjustable to various types of backplane connectors.
3. First investigation of a combined system solution for equalization and NEXT noise cancellation for 20-Gbit/sec backplane transmission.
4. Representation of a systematic work flow to develop system/IC solution for backplane channel effects.
5. First examination of the feasibility of 4-PAM as an alternative signaling scheme for 20-Gbit/sec transmission in legacy backplane environment.

This dissertation is organized as follows. Chapter 2 describes the details of the primary challenges in legacy backplane signaling environment and their impacts on the signal integrity. Broadband backplane channel measurement methodology and behavioral channel modeling are introduced. Based on the channel model, multi-level signaling was investigated and compared to conventional Non-Return-to-Zero (NRZ) signaling to realize reliable transmission of 20-Gbit/sec throughput. In chapter 3, a system architecture is suggested for equalization and NEXT noise cancellation for 20-Gbit/sec backplane transmission. Historical background and comparison of topologies for equalization and noise cancellation techniques are provided. Moreover, the optimum structure and specification of each building block are derived through a system simulation. Chapter 4 is focused on the circuit design and implementation of the suggested equalizer and NEXT noise canceller. The transistor-level building blocks are described in detail. The effort to overcome the intrinsic challenges of 0.18-um CMOS process technology is introduced. The simulated and measured results are represented. In chapter 5, conclusion and future work of this dissertation are provided.

CHAPTER II

BACKPLANE TRANSMISSION ENVIRONMENT

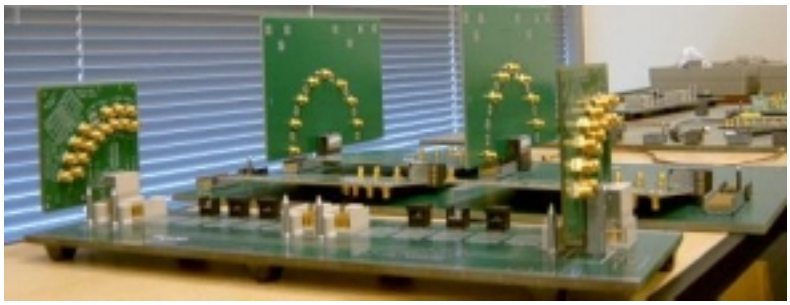
Legacy backplanes were designed to transfer hundreds of megabits of data per second. Conventional connectors, through-hole vias, and inexpensive FR4 laminates were more than enough for those speeds. However, bandwidth-hungry telecommunication and data-communication industries have been raising this transfer rate up to multi-Gbit/sec in these legacy backplanes. The multi-Gbit/sec data transmission leads to the challenging channel issues in the legacy backplanes. This chapter describes the primary challenges of the backplane signaling environment– loss and crosstalk noise in detail. Then, backplane channel measurement and characterization method are introduced. Based on the measured backplane channel characteristics, the feasibility of multi-level signaling is investigated as an alternative signaling scheme rather than conventional NRZ signaling.

2.1. BACKPLANE CHANNEL CHARACTERISTICS

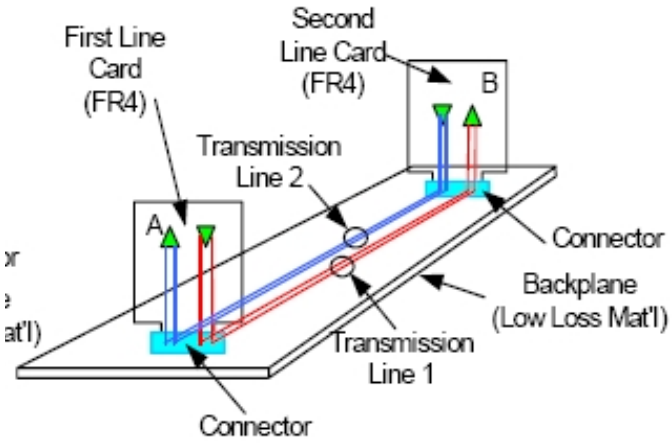
2.1.1 BACKPLANE SIGNALING CONFIGURATION

The backplane link is a high speed differential, point-to-point serial link between a chip on a line card and a chip on another line card connected through a backplane. Figure 2.1 shows the picture and the conceptual illustration of a typical backplane signaling environment. The high-speed transceiver chipsets are mounted on the line cards. These line cards are plugged into the PCB backplane board through these high-speed connectors.

The multi-Gbit/sec data signals are transmitted through the parallel PCB traces on the backplane. In this signaling environment, the passive physical components are the line card and line card packages, backplane PCBs, and the backplane connectors. The FR4 is widely used dielectric material in the legacy backplane boards. Thus, this work is focused on the characterization of the FR4 backplane channel.



(a)



(b)

Figure 2.1. (a) Picture of a typical backplane channel. (b) Illustration of backplane signaling environment.

The electrical parameters that affect the channel response and influence the design of various components in the backplane link are reflections, loss and crosstalk. The loss is composed of conductor and dielectric loss. The conductor loss has two components: DC loss and the skin effect loss which is proportional to square-root of frequency. The dielectric loss is proportional to frequency and thus becomes severe in the microwave frequency range (i.e. beyond 1 GHz) for FR4 dielectric based components. This channel loss characteristic induces the signal power dispersion and affects the link performance severely. Thus, the channel loss is a major noise factor in the multi-Gbit/sec backplane signaling environment.

Crosstalk noise occurs when signals are coupled between adjacent pins in connectors, and can be categorized as NEXT and FEXT. NEXT noise has a high pass filter frequency response. Meanwhile, FEXT experiences channel loss. Thus, FEXT has very small magnitude and negligible effects compared to NEXT. The transmitted signal is coupled to the neighboring receivers through the NEXT noise channel. As data rate increases, this NEXT noise affects the adjacent signal's integrity more severely. Therefore, NEXT noise becomes another major noise component of the legacy backplane environment.

Meanwhile, reflections are caused by impedance discontinuities along the channel. These reflections reduce the signal amplitude delivered to the receiver and cause resonance dips in the channel transfer function. Impedance discontinuities can be seen at any point along the path between the transmitter and the receiver; e.g., the interface between connectors, vias between different signal layers, and all other transitions from a connector to the PCB. The primary effect of an impedance discontinuity is reflection of the signal energy back to the source. This reflected signal power is added or subtracted

from the input signal and leads to the signal quality degradation. This impact of the reflection can be addressed by the back-drilled via structure. This work is focused on two primary noise components : loss and coupling noise.

2.1.2 BACKPLANE CHANNEL LOSS

As high speed I/O interface technology evolves, resistive loss affects the link performance by decreasing the signal amplitude and slowing edge rates. The primary origins of this loss are DC loss, skin effect and dielectric loss are described in the following sections.

2.1.2.1) DC loss

A DC loss depends on the resistivity of the conductor and the total area in which the current is flowing. The resistive loss can be calculated as in eq. (2.1).

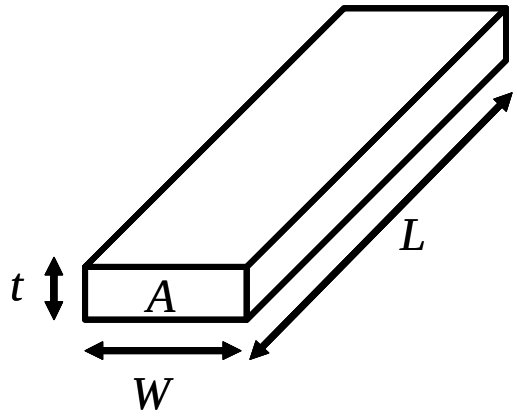


Figure 2.2. Resistive conductor

$$R = \frac{\rho L}{A} = \frac{\rho L}{Wt} \qquad \text{eq. (2.1)}$$

,where R is the total resistance of the line, ρ the resistivity of the conductor material in ohm-meters (the inverse of conductivity), L the length of the line, W the conductor width, t the conductor thickness, and A the cross-sectional area of the signal conductor.

Since the dielectric materials used in PCBs are not perfect insulators, there is a dc loss associated with the resistive drop across the dielectric material between the signal conductor and reference plane. The dielectric losses at dc (it is not just at DC but through the frequency span) for commercial PCB substrate are usually negligible and can be ignored.

2.1.2.2) Skin effect

Skin effect is a physical phenomenon related to high frequency transmission on a wire. Beyond tens of MHz, the electromagnetic field of the wire causes most of the electrical current to become crowded at the edges of the wire. This phenomenon alters the distribution of the signal current throughout the wire and changes the effective resistance of the wire. The current flowing in a conductor will migrate toward the periphery or ‘skin’ of the conductor. This is the origin of the name ‘skin effect’. The resulting effect is the increased signal attenuation at higher frequencies.

Skin effect manifests itself primarily as resistance and inductance variations. As frequency increases, the non-uniform current distribution in the transmission line causes the resistance to increase with the square-root of frequency and the total inductance to fall asymptotically toward a static value called the external inductance.

In the microstrip transmission line, the electric and magnetic fields intersect the signal trace or the ground plane conductor. They will penetrate the metal and their amplitudes

will be attenuated. The amount of attenuation will depend on the resistivity ρ of the metal and the frequency content of the signal. The amount of penetration into the metal, known as the skin depth is shown in eq. (2.2).

$$\sigma = \sqrt{\frac{2\rho}{\varpi\mu}} = \sqrt{\frac{\rho}{\pi f\mu}} \qquad \text{eq. (2.2)}$$

,where ϖ and μ are the angular frequency and the permeability of free space, respectively.

2.1.2.3) Dielectric loss

As frequency increases over 1 GHz, dielectric loss becomes another dominant loss factor in the legacy backplane applications. When dielectric loss is accounted for, the dielectric constant of the material becomes a complex value as shown in eq. (2.3).

$$\varepsilon = \varepsilon^{'} - j\varepsilon^{''} \qquad \text{eq. (2.3)}$$

,where the imaginary portion represents the loss and the real portion is the typical value of the dielectric constant. Since the imaginary portion of eq. (2.3) represents the loss, it is convenient to think of it as the effective conductivity of lossy dielectric.

Subsequently, $1/\rho = 2\pi f\varepsilon$ becomes an equivalent loss mechanism, where ρ is the effective resistivity of the dielectric material and f is frequency. The typical method of loss characterization in dielectrics is by the loss tangent shown in eq. (2.4).

$$\tan|\delta_d| = \frac{1}{2\rho\pi f\varepsilon} = \frac{\varepsilon^{''}}{\varepsilon^{'}} \qquad \text{eq. (2.4)}$$

Figure 2.3 shows the overall loss transfer function of the FR4 legacy backplane channel. The dielectric loss increases and becomes the major loss factor as well as the conductor loss beyond 1 GHz. The resulting overall channel loss drastically increases and

the corresponding frequency response is similar to that of a typical low-pass filter. Thus, the multi-Gbit/sec signal experiences the loss of the high-frequency components through the backplane. The following section describes the impacts of this channel loss on the signal integrity performances.

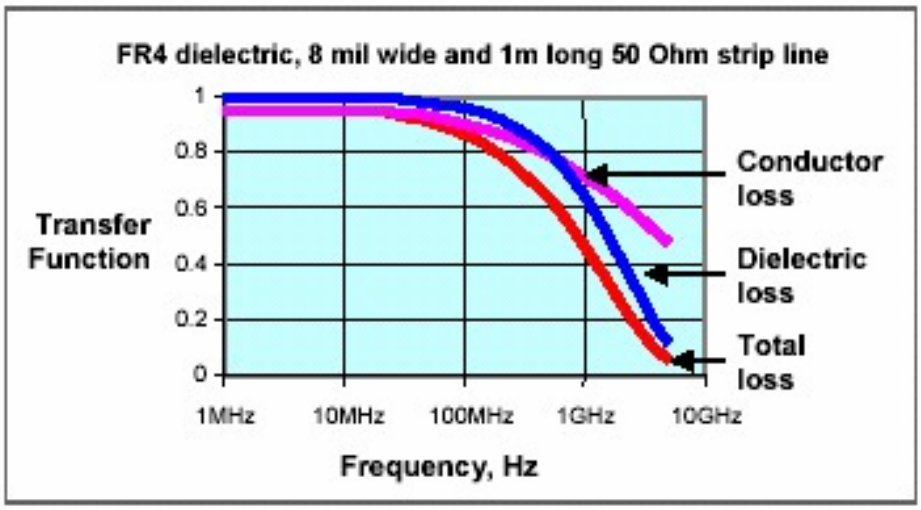


Figure 2.3. Loss transfer functions of FR4 legacy backplane

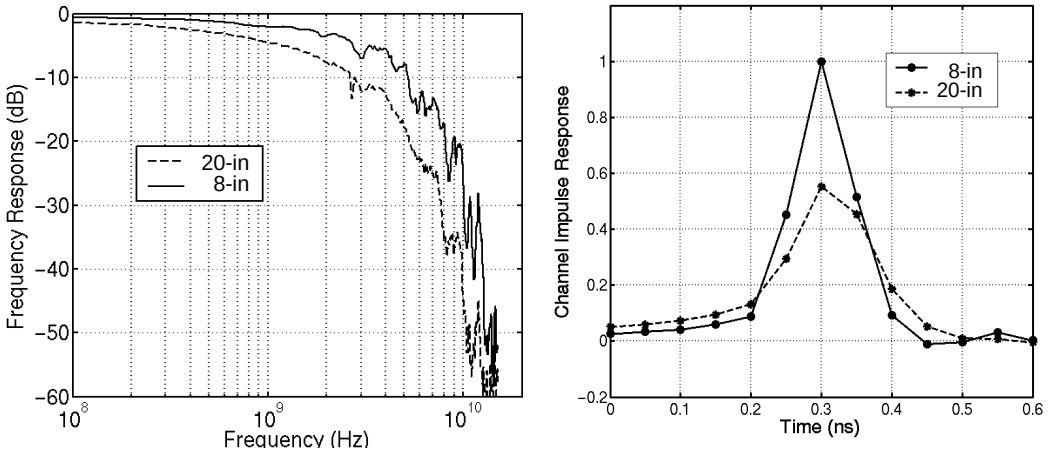
2.1.2.4) Impacts of channel loss on the signal integrity

Fourier series represents the spectral contents of a periodic time-domain signal. Wideband digital signals can be approximated to a square-wave pulse train. The Fourier series expansion of this square-wave pulse train contains many frequency components as shown in eq. (2.5).

$$f(x) = \frac{2}{\pi} \sum_{n=1,3,5,\ldots} \frac{1}{n} \sin(2\pi n f x) \qquad \text{eq. (2.5).}$$

,where f is the frequency and x is the time. The backplane channel loss characteristics are frequency-dependent. Specifically, high frequency components of the input signal

experience larger loss than the lower frequency components around DC. This high frequency loss becomes worse in longer backplane channel environment, as shown in Figure 2.4. Figure 2.4(a) shows that a 20-in FR4 backplane has much larger attenuation or loss compared to an 8-in FR4 backplane. The resulting impulse response of the 20-in FR4 backplane has more power loss and more widened pulse shape compare to 8-in channel, as shown in Figure 2.4(b).



(a) (b)

Figure 2.4. Forward transmission channel for 8-in and 20-in FR4 backplane. (a) Frequency responses and (b) impulse responses.

When the signal goes through the dispersive backplane channel with the impulse response, shown in Figure 2.4(b), its output signal power spreads in time. This spreading of signal power causes ISI. In other words, transmitting a square pulse through such a dispersive channel results in a widened and flattened pulse at the far end. This implies that each data bit of information overlaps with its adjacent bits. This overlap can cause major distortions of the signal. As data rate and channel length increase, the ISI can be so

severe that it becomes impossible to recover the original transmitted data. This is a major phenomenon limiting the maximum speed, and must be addressed beyond 5-Gbit/sec data rates in the legacy backplane channels longer than 20 inches.

Figure 2.5(a-c) show how ISI affects the signal integrity performance of a 5-Gbit/sec NRZ signal. When a clean 5-Gbit/sec NRZ signal, as illustrated in Figure 2.5(a), propagates through a 8-in and 20-in backplane board traces, its eye becomes smaller and almost closed due to ISI, as shown in Figure 2.5(b) and (c), respectively.

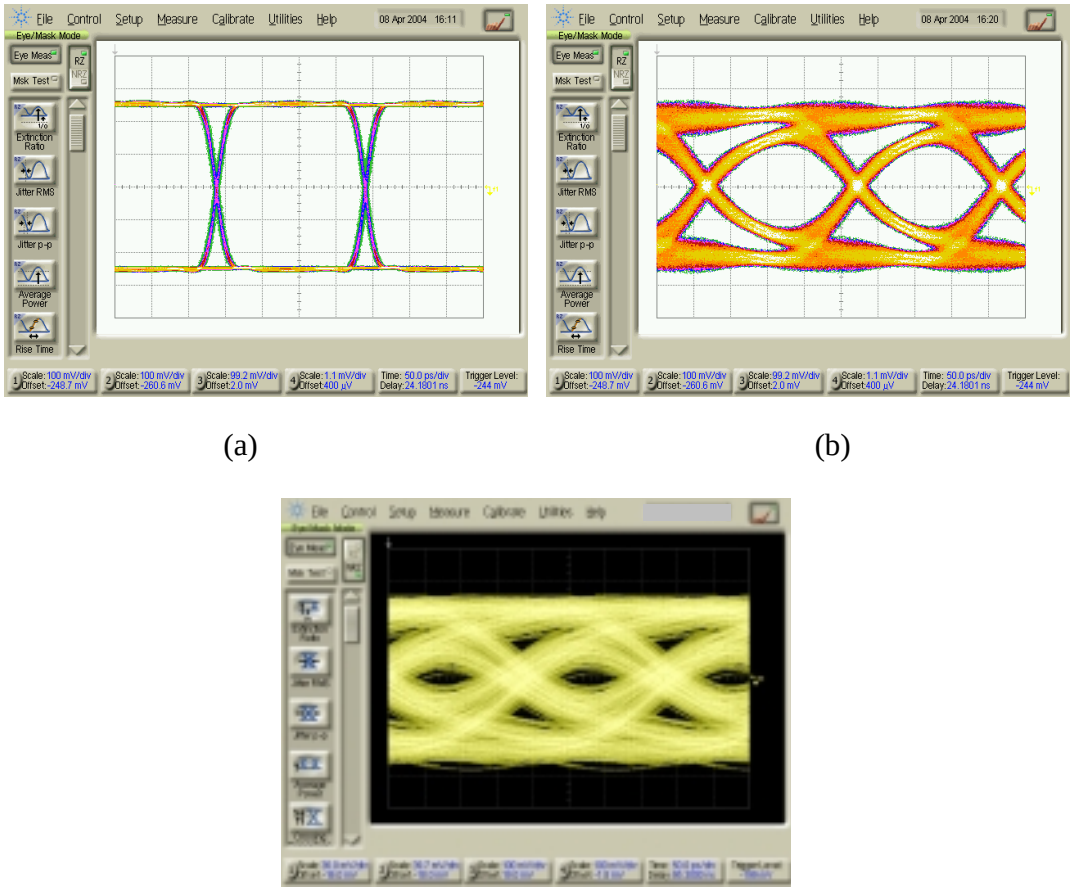
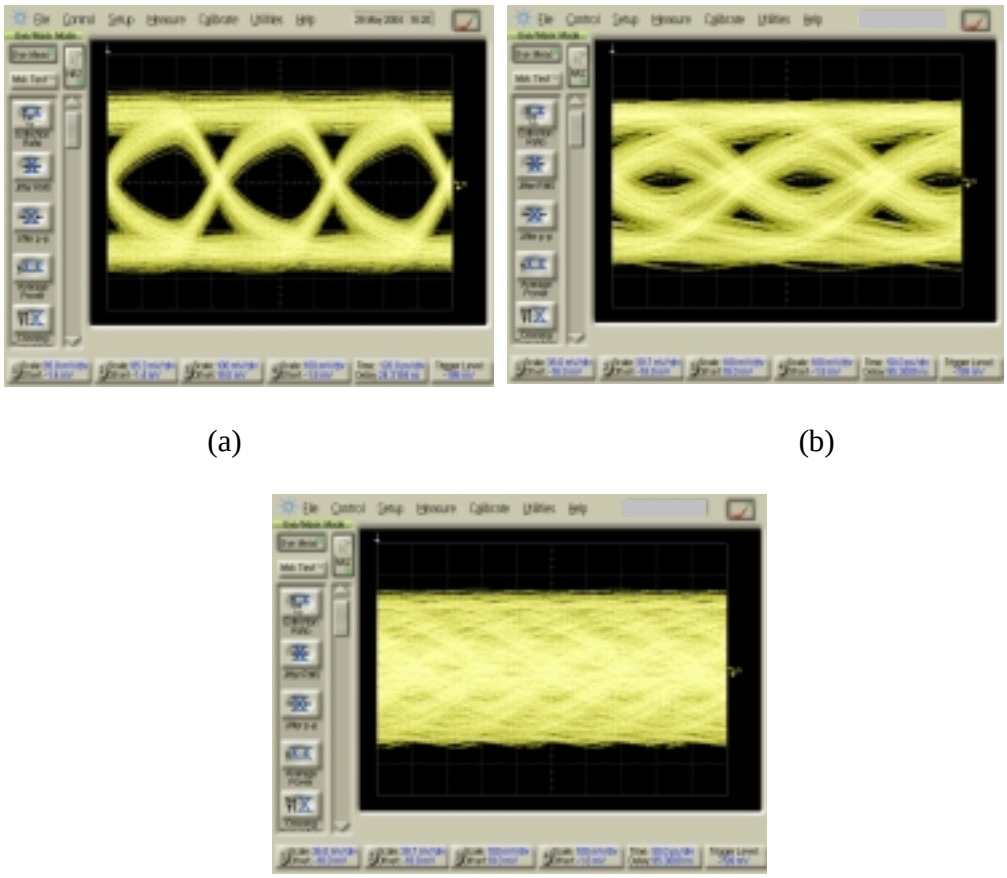


Figure 2.5. Eye diagrams of 5-Gbit/sec NRZ signals of (a) clear input signal, (b) output signal of 8-in backplane trace, and (c) output signal of 20-in backplane trace.

Figure 2.6(a-c) show the eye diagrams of backplane channel output signals of the 2.5-, 5-, and 10-Gbit/sec NRZ signal over 20-in FR4 backplane channel. The 2.5-Gbit/sec NRZ signal has large eye opening at the backplane output enough to provide reliable link performance. Meanwhile, beyond 5-Gbit/sec, the resulting backplane output signal becomes severely impaired, as shown in Figure 2.6(b) and (c).



(a) (b)

(c)

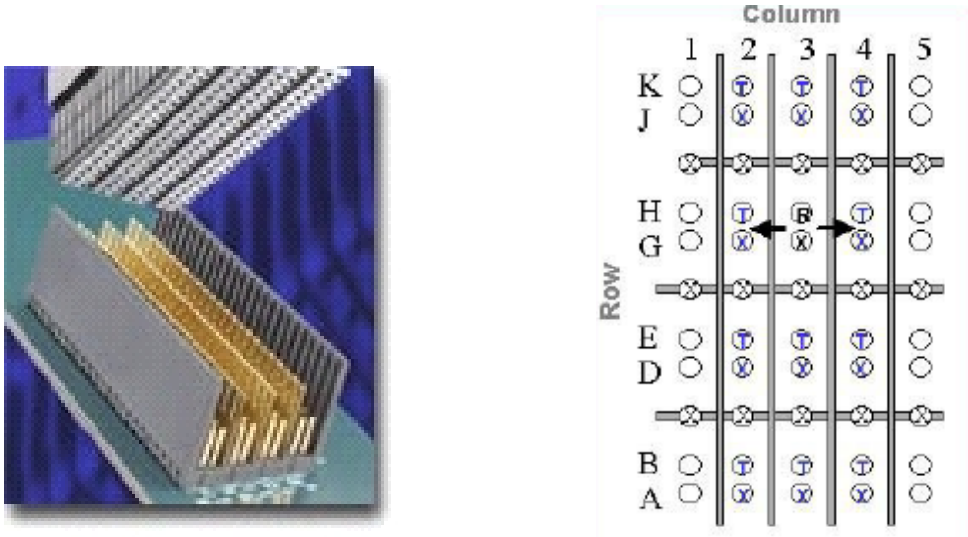
Figure 2.6. Eye diagrams 20-in FR4 backplane channel output signal of (a) 2.5 Gbit/sec, (b) 5 Gbit/sec and (c) 10 Gbit/sec.

As shown in Figure 2.5 and Figure 2.6, the NRZ signal transmission beyond 5 Gbit/sec turns out to be very challenging over 20-in FR4 backplane channel. Thus, channel loss

compensation technique is essential to increase the maximum data throughput in the legacy backplane signaling environment. Moreover, an alternative signaling scheme can be applied to lessen the effect of the channel loss.

2.1.3 CROSSTALK CHANNEL CHARACTERISTICS

The line cards are plugged into backplane PCB through backplane connectors. These connectors have several tens of signal pins packed very densely as shown in Figure 2.7. As the data speed increases, the frequencies of the signal's spectral content are ranging from several GHz up to tens of GHz. This high frequency signal component is coupled through the connector pins. Meanwhile, the legacy backplane has not been designed with consideration of this coupling effect for the signal integrity. Thus, this coupling effect or crosstalk noise becomes one of the serious noise factors in the multi-Gbit/sec application over legacy backplanes.



(a) (b)

Figure 2.7. Backplane connector. (a) Picture and (b) signal pin configuration of the backplane connector

2.1.3.1) Near-end crosstalk (NEXT) channel

The crosstalk noise is categorized as the NEXT and the FEXT, as shown in Figure 2.8. The NEXT channel has a high-pass frequency response in general. The adjacent transmit signal is coupled to the neighboring signal pins with the NEXT channel characteristic. This transmit signal power is much larger than the received signal power, which experiences the backplane channel loss. This NEXT noise is coupled and induces jitter impairment to the neighboring channel's signal. Since the NEXT channel has high-pass filter (HPF) frequency response, adjacent transmit signal power affects more seriously as its data speed or bandwidth increases. Meanwhile, the origin of the FEXT is the input signal power to the adjacent receiver. This FEXT noise experienced the backplane channel loss before being coupled to the neighboring signal pins. The resulting FEXT noise has negligible power level to affect the signal integrity compared to the NEXT noise. Therefore, this work is focused on the NEXT channel characteristics and its impacts on the signal integrity.

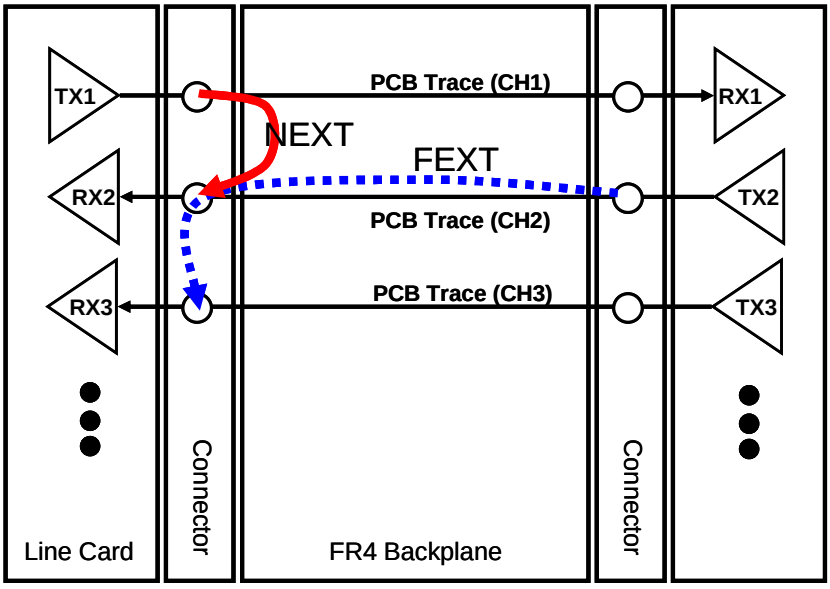
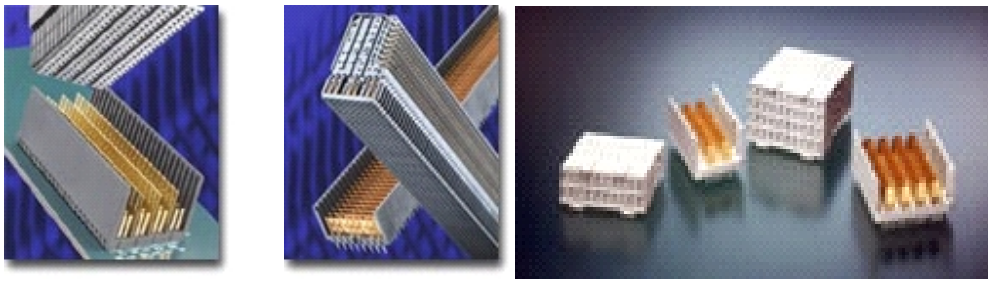


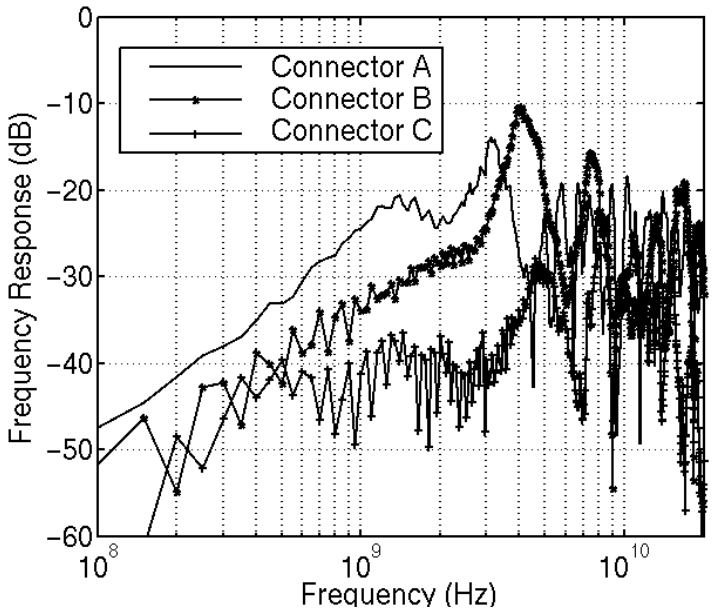
Figure 2.8. The backplane signaling configuration.

Since this NEXT is the coupling phenomenon between the signal pins in the connector, the NEXT channel characteristic depends on the geometry of the connector. Figure 2.9(a) and (b) show three typical backplane connectors (i.e. type A - GBX, type B - HSD, and type C - HM-ZD) and the corresponding measured NEXT channel responses, respectively. The connector A, B, and C have the corner frequency values of 3, 4, and 5 GHz, respectively.



Type A (GBX) Type B (HSD) Type C (HM-ZD)

(a)



(b)

Figure 2.9. (a) Picture of backplane connectors (GBX, HSD, and HM-ZD). (b) NEXT noise channel for these three different types of connectors.

2.1.3.2) NEXT noise impact on signal integrity

In order to illustrate the NEXT effect on the signal integrity, backplane signaling environment is modeled as shown in Figure 2.10. The coupling noise source is an aggressor. The data dependent noise, i.e. NEXT noise, from this aggressor is coupled to the received 'victim' signal. In the shown backplane signaling environment, the ISI and the NEXT noise are dominant noise factors rather than the thermal noise. Therefore, the corresponding SNR is defined as in eq. (2.6).

$$SNR = \frac{SignalPower}{NoisePower} = \frac{S}{N} = \frac{S}{(N_{ISI} + N_{NEXT})} \qquad \text{eq. (2.6)}$$

,where N_{ISI} and N_{NEXT} are noise power due to ISI and NEXT effects, respectively.

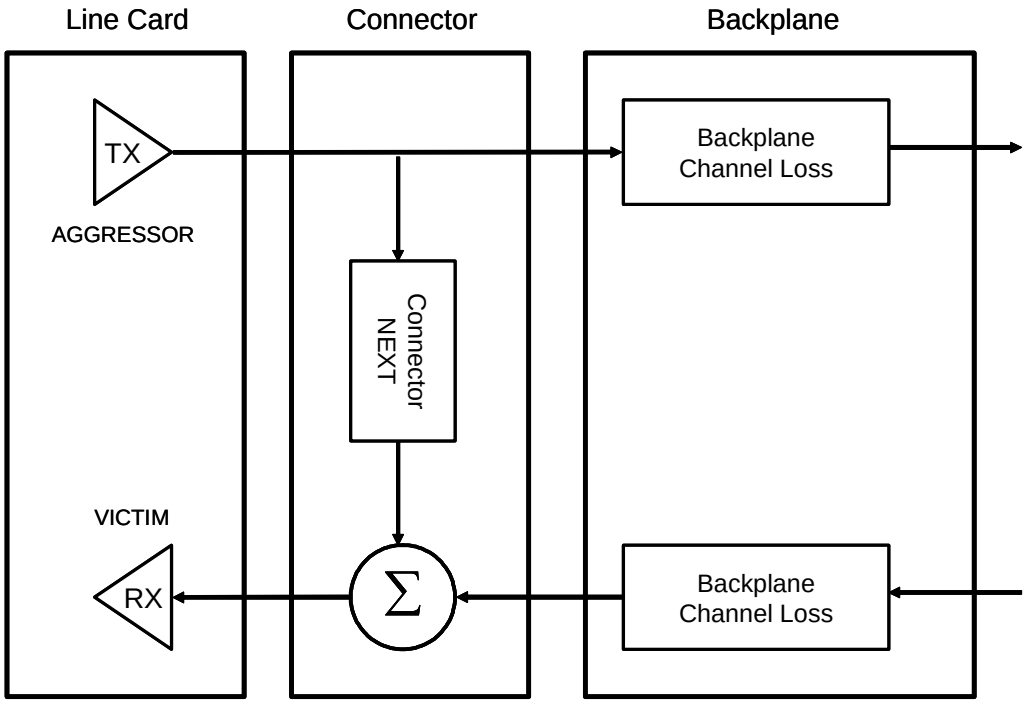


Figure 2.10. Behavioral model of the backplane signaling environment.

The backplane channel loss and NEXT channel have a low-pass and high-pass response, respectively. These two channel frequency responses cross each other at the certain frequency depending on pin spacing and geometry, as shown in Figure 2.11. As the data speed increases, the victim signal power S decreases. Meanwhile, the effects of the ISI and NEXT, i.e. N_{ISI} and N_{NEXT}, are increasing. Thus, the resulting SNR decreases drastically and the backplane signaling environment becomes more challenging for the multi-Gbit/sec application.

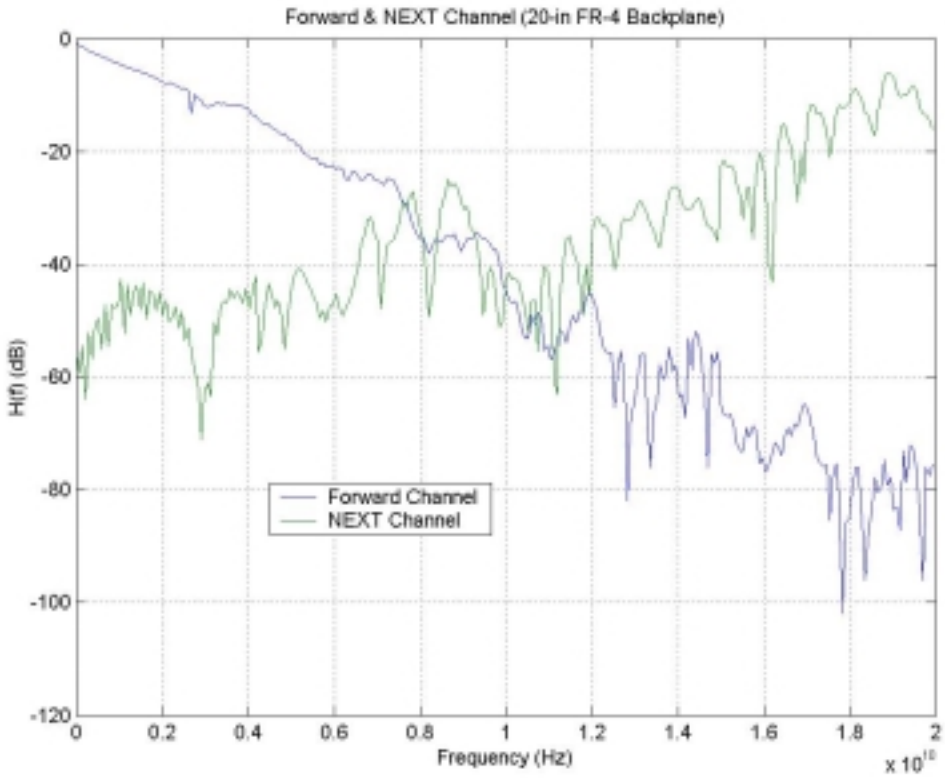
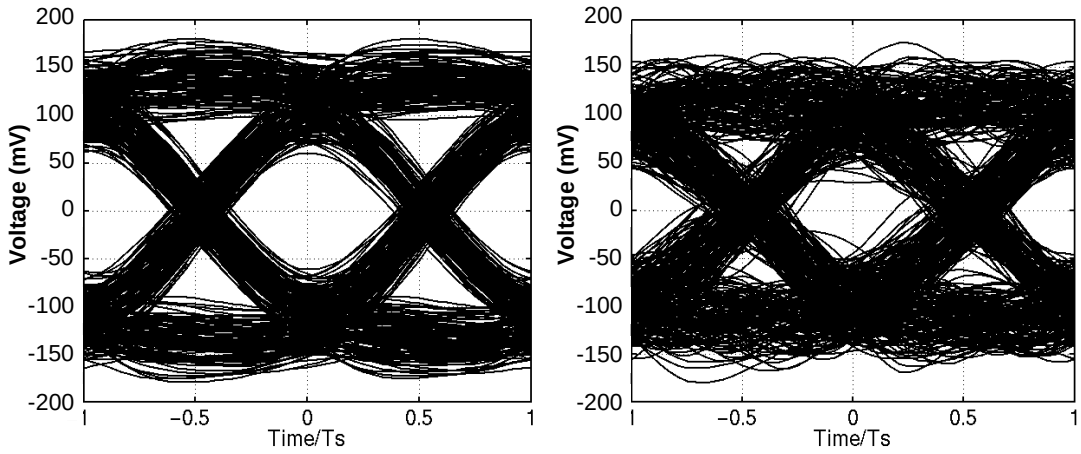


Figure 2.11. The frequency responses of the NEXT and loss characteristics for 20-in FR4 backplane.

Figure 2.12 shows the NEXT effect to the signal integrity after the channel loss is compensated. Due to the NEXT noise effect, the eye diagram shown in Figure 2.12(b) has more jitter noise than that shown in Figure 2.12(a). This increased jitter noise can corrupt the overall link quality. In order to alleviate this NEXT noise, sophisticated connectors and signal processing technique has been proposed [5], [6]. However, these techniques cannot be applied to legacy backplanes because this would involve replacing the entire backplane. Thus, this work suggests an active NEXT noise cancellation technique to reduce the NEXT noise effect.



(a) (b)

Figure 2.12. The eye diagrams of 10-Gbit/sec NRZ signal after channel loss compensated (a) without and (b) with a aggressor signal.

2.2. BACKPLANE CHANNEL CHARACTERIZATION

The backplane channel is very challenging environment for the multi-Gbit/sec transmission. In order to realize reliable link performance, signal processing techniques

to compensate or remove the channel effects are required. To devise and optimize these signal processing techniques, the actual channel characteristics are utilized. Thus, accurate channel measurement and its corresponding analysis are essential for the realization of reliable backplane link beyond multi-Gbit/sec. The following sections introduce high-speed backplane channel measurement methodologies and the behavioral channel modeling technique applied in this work.

2.2.1. HIGH-SPEED BACKPLANE CHANNEL MEASUREMENT

Two choices are available to design and extract measurement-based channel models with either a differential Time Domain Reflectometer (TDR) or a 4-port Vector Network Analyzer (VNA). Each has unique advantages. TDRs provide more straight-forward channel characteristics while VNAs produce more accurate and traceable results. In this work, s-parameter measurement method was adopted to derive the channel impulse response. The following sections describe the details of each measurement methodology.

2.2.1.1) Time-Domain Reflectometry (TDR)

TDR measurements are common for PCB board characterization. The key advantage of the TDR over frequency-domain measurements is the ability to extract electrical data relevant to digital systems, which represent time-domain signals. Digital signal represent wide bandwidth signals, not single frequencies as common in typical microwave designs. Extracting channel data in the time domain provides voltage-time data that relate back to system operation. The TDR can extract the following channel characteristics; impedance, velocity, and mutual and self-transmission line electrical parameters.

A TDR combines a sampling oscilloscope with a step generator capable of launching a fast edge into the Device Under Test (DUT), as shown in Figure 2.13. The time, location and magnitude of the reflected wave provide an easy interpretation to display impedance discontinuities vs. distance. The transmitted wave enables the measurement of propagation delay and signal deterioration due to system loss and reflections.

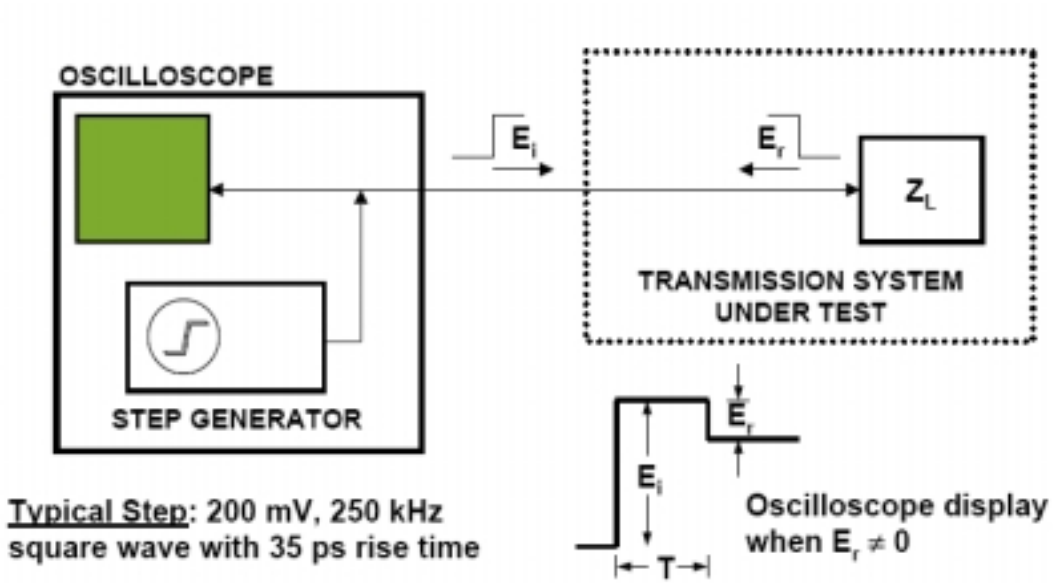


Figure 2.13. Conceptual illustration of TDR operation

The TDR uses basic transmission line theory by measuring the reflection of an unknown device relative to the known standard impedance. This is based on knowing the energy transmitted through any discontinuity will result in energy being reflected back. The reflection magnitude will be a function of both transmitted and the magnitude of the impedance discontinuity. The time delay between transmitted and reflected energy will be a function of distance and propagation velocity.

Impedance information is extracted by calculating the reflection coefficient ρ, as a function of the incident and reflected voltages. Using the TDR reference characteristic impedance and ρ, the trace characteristic impedance can be computed using the eq. (2.7) and eq. (2.8).

$$Z_{DUT} = Z_o \frac{1+\rho}{1-\rho} \qquad \text{eq. (2.7)}$$

$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{DUT} - Z_o}{Z_{DUT} + Z_o} \qquad \text{eq. (2.8)}$$

These equations are used to calculate the trace impedance Z_{DUT}, where Z_0 represents the output impedance of the TDR. The oscilloscope will calculate the value of ρ to determine the trace impedance. Figure 2.14 shows the example of the backplane channel measurement using the TDR.

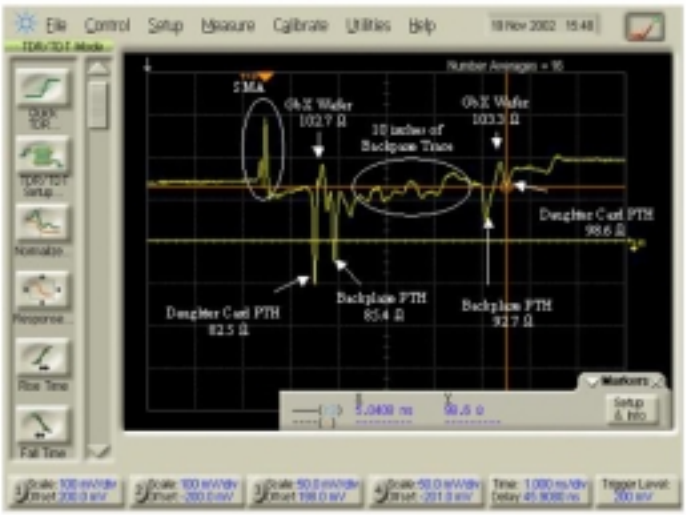


Figure 2.14. The example of the backplane channel measurement using the TDR.

2.2.1.2) 4-port Vector Network Analyzer (VNA)

A VNA uses stimulus to characterize the DUT. A sine wave is transmitted into the DUT while tuned receivers are swept in lockstep, providing both reflection and transmission properties. The VNAs, shown in Figure 2.15, offer greater measurement resolution and accuracy than a TDR through calibration and fixture removal techniques. These VNA measurements are often expressed as scattering parameters (or S-parameters) that can be translated into time domain views.

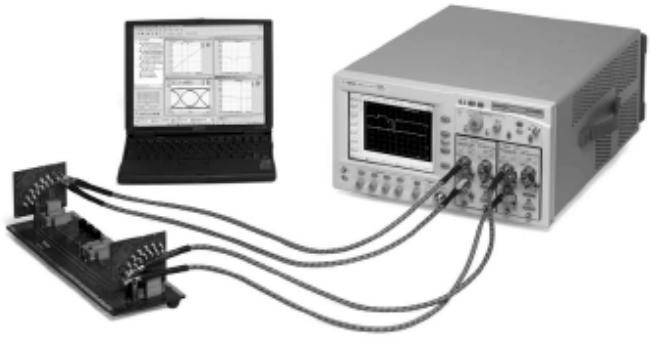


Figure 2.15. 4-port differential-ended VNA system

The 4-port device, shown in Figure 2.16(a), can be the simplest case which adjacent PCB traces are operating in a single-ended fashion. When these two traces are located within relatively close proximity to each other on a backplane, coupling phenomena occur. The matrix shown in Figure 2-16(b) provides the 16 single-ended s-parameters that are associated with these two lines.

(a)

$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$

(b)

Figure 2.16. (a) 4-port single-ended DUT and (b) the resulting s-parameter matrix.

Once the single-ended s-parameters have been measured, it is desirable to transform these to balanced s-parameters to characterize differential devices. This mathematical transformation is possible because a special condition exists when the DUT is a linear and passive structure. Linear passive structures include PCB traces, backplanes, cables, connectors, IC packages and other interconnects. Utilizing linear superposition theory, all of the elements in the single-ended s-parameter matrix, shown in Figure 2-16(b), are processed and mapped into the differential s-parameter matrix shown in Figure 2.17(b).

(a)

$$\begin{bmatrix} S_{DD11} & S_{DD12} & S_{DD13} & S_{DD14} \\ S_{DD21} & S_{DD22} & S_{DD23} & S_{DD24} \\ S_{DD31} & S_{DD32} & S_{DD33} & S_{DD34} \\ S_{DD41} & S_{DD42} & S_{DD43} & S_{DD44} \end{bmatrix}$$

(b)

Figure 2.17. Balanced s-parameters of a differential device

Interpreting the large amount of data in the 16-element differential s-parameter matrix is helpful to analyze one quadrant at a time. The first quadrant in the upper left of Figure 2.18 is defined as 4 parameters describing the differential stimulus and differential response characteristics of DUT. This is the actual mode of operation for most high-speed differential interconnects, so it is typically the most useful quadrant that is analyzed first. It includes input differential return loss (SDD11), forward differential insertion loss (SDD21), output differential return loss (SDD22) and reverse differential insertion loss (SDD12).

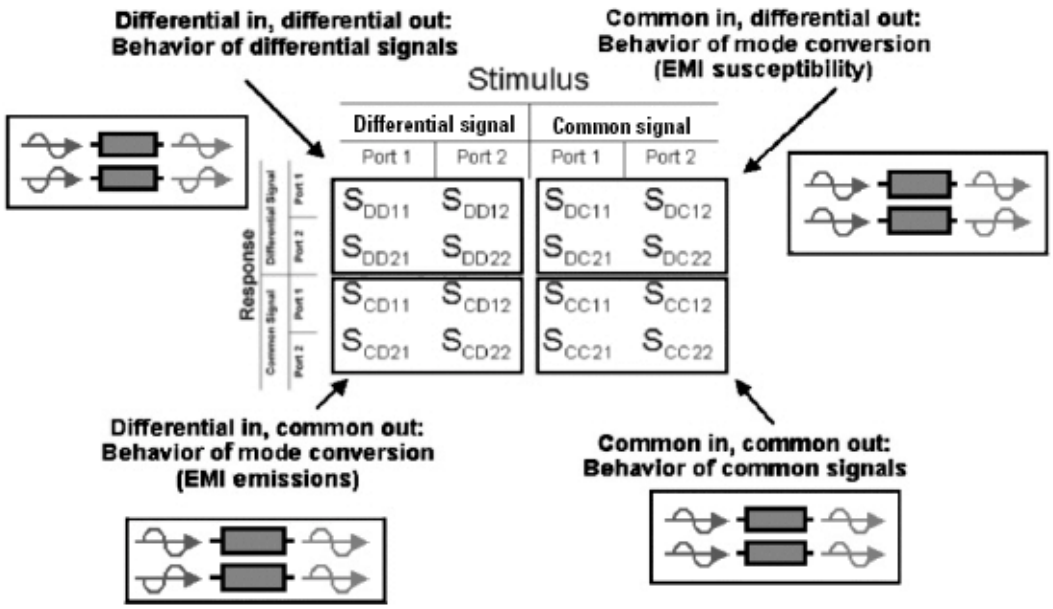


Figure 2.18. 16-element differential s-parameter matrix.

2.2.2. BACKPLANE CHANNEL BEHAVIORAL MODELING

The optimum modulation scheme and equalizer specifications can be derived from the loss characteristic of the backplane channel and the channel SNR, i.e. the value of the SNR at each particular frequency. Clearly, the channel SNR is impacted by the spectral distribution of the noise. The primary source of noise in high-speed backplane communications is the NEXT noise. Because both the channel frequency response and the noise spectrum cannot be accurately characterized with a trivial model, a thorough analysis of channel characteristics is essential to optimize the system design parameters and to devise methods to improve signal quality.

The complex-valued frequency domain channel transfer functions, H(f) shown in eq. (2.9), can be measured using the VNA.

$$H(f_k) = \sum_{k=0}^{N-1} \left| S_{21}(f_k) \right| e^{j2\pi f_k} \quad \text{, where } f_k = k\left(\frac{BW}{N}\right) \qquad \text{eq. (2.9)}$$

To obtain real-valued impulse response r(t) from the complex-valued channel data H(f), complex conjugate symmetry of H(f) is appended eq. (2.10).

$$H(f_k) = H^*(f_{2N-k}) \quad \text{, where } k = 0 \sim (2N-1) \qquad \text{eq. (2.10)}$$

By taking the 2N-point Inverse Fourier Transform (2N-IFT) for the extended channel data eq. (2.11), a real-valued impulse response with sample spacing of (0.5/BW) is obtained.

$$h(t) = IFT\left(\sum_{k=0}^{2N-1} H(f_k)\right) = \sum_{m=0}^{2N-1} h_m \delta(t - m\Delta t) \text{ ,where } \Delta t = 0.5/BW \text{ (sec)} \qquad \text{eq. (2.11)}$$

Figure 2.19(a), (b), and (c) show the 20-in FR4 backplane channel loss characteristic, the corresponding complex-conjugated response and the resulting real-valued impulse response, respectively.

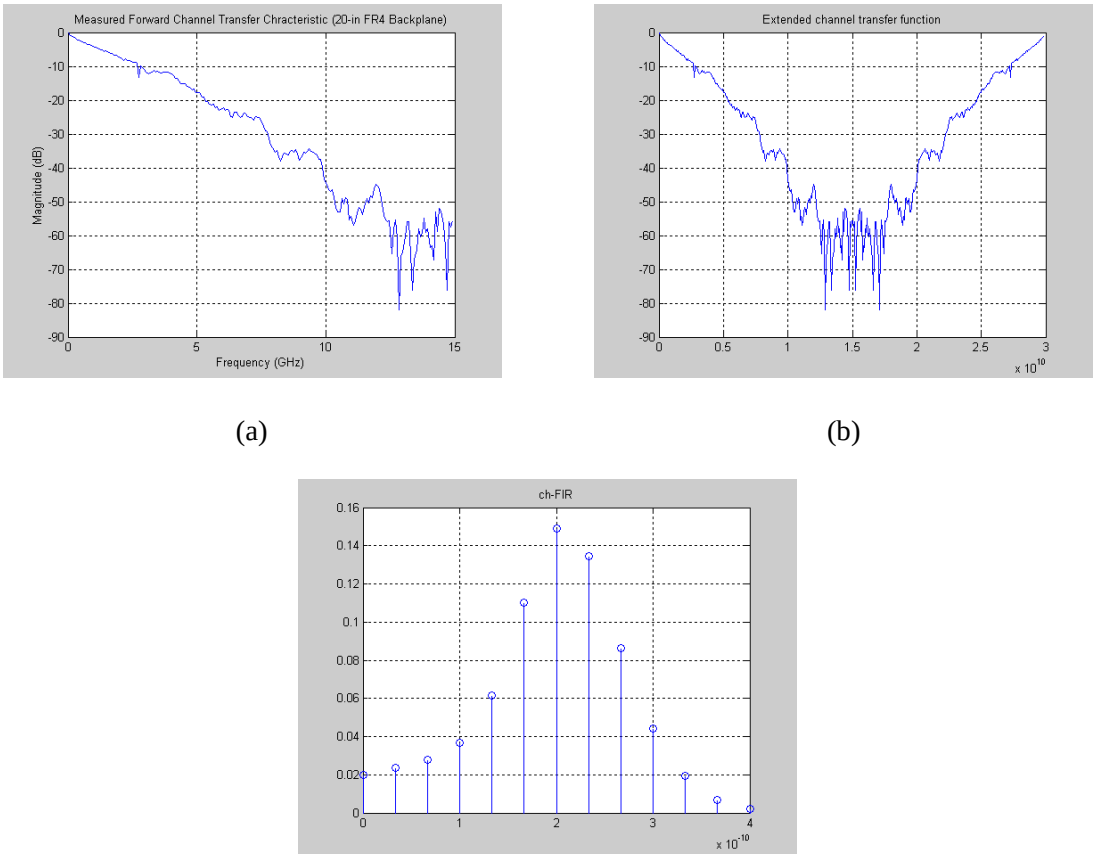


Figure 2.19. System channel modeling using measured channel data: (a) Measured complex-valued channel data, (b) the corresponding complex conjugate symmetry, and (c) real-valued impulse response with (0.5/BW) sample interval

2.3. ALTERNATIVE SIGNALING SCHEME

Various modulation schemes such as binary NRZ, M-PAM, M-Quadrature Amplitude Modulation (QAM), and Discrete Multi-Tone (DMT) can be considered as candidates for signaling schemes over backplane channels. M-QAM requires frequency conversion procedures and the corresponding carrier recovery process result in the increase of implementation complexity. DMT signal conveys multi-carrier modulated waveforms with a very high peak-to-average power ratio which results in excessive linearity

requirements for Analog-to-Digital Converters (ADCs) and amplifiers. NRZ and M-PAM modulation schemes are considered most practical in terms of implementation complexity and error performances [12, 13]. These modulation schemes are compared based on the frequency dependent characteristics of the forward transmission and the NEXT channel coupling for a 20-in FR4 backplane.

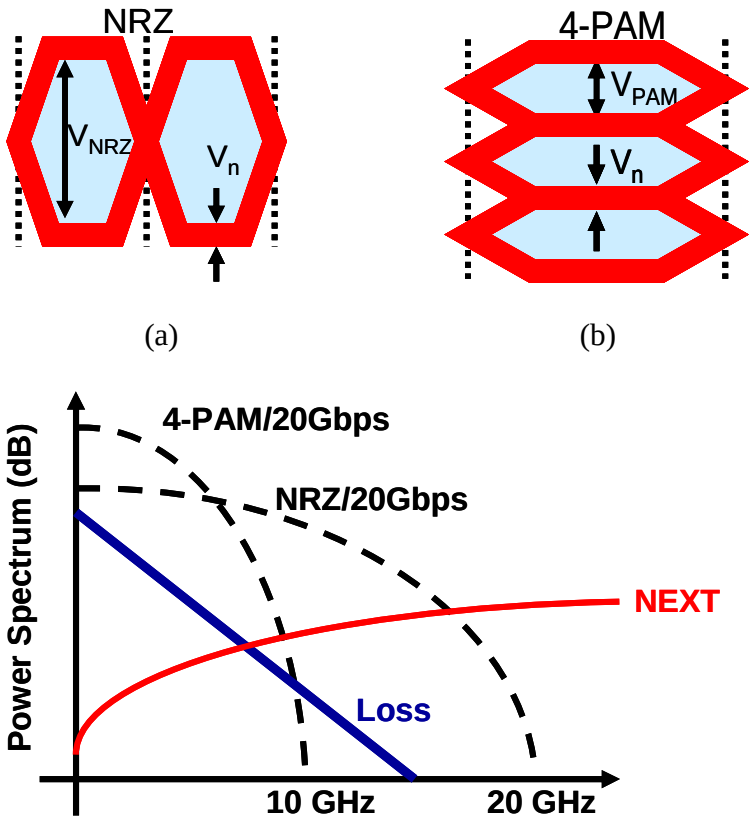


Figure 2.20. The eye diagrams of (a) NRZ, (b) 4-PAM signaling, and (c) comparison of the corresponding spectrums.

Multilevel signaling has better spectral efficiency than binary NRZ signaling because each symbol encodes more than one bit. In severely lossy channels, multilevel signaling

experiences less channel loss and NEXT noise than NRZ signaling. A 4-PAM has twice the spectral efficiency of NRZ signaling because it delivers two bits in one symbol. However, this 4-PAM signal has a 9.5 dB SNR penalty as compared to NRZ signals, because its eye opening is 1/3 of that of an NRZ signal. Therefore, 4-PAM signaling is preferred to NRZ signaling when it overcomes this SNR penalty by suffering less channel loss than NRZ [14].

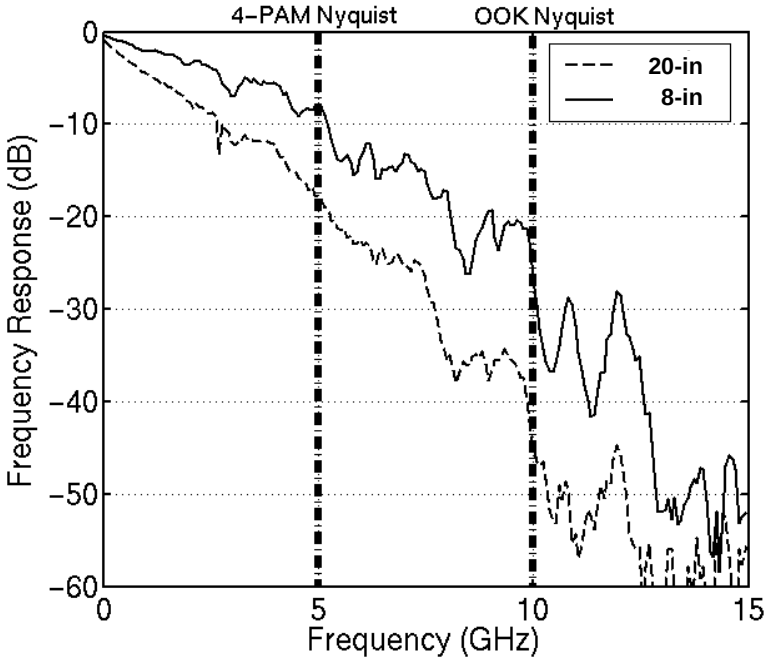


Figure 2.21. Frequency responses of 8-, 20-in FR4 backplane channels

20-Gbit/sec throughput NRZ and 4-PAM signals have Nyquist frequencies at 10 GHz and 5 GHz, respectively. These Nyquist frequencies are marked on the forward responses of 8- and 20-in FR4 backplane traces, as shown in Figure 2.21. The difference in channel loss between NRZ and 4-PAM is 17 and 28 dB for 8- and 20-in backplane channels,

respectively. As a result, 4-PAM has the corresponding SNR margins of 7.5 and 18.5 dB compared to NRZ signaling. Moreover, 4-PAM signaling experiences less NEXT noise effect because its signal bandwidth is half that of an NRZ signal. Therefore, a 4-PAM signaling scheme is adopted for 20-Gbit/sec data transmission over FR4 backplane I/O channels.

CHAPTER III

SYSTEM STUDY

Backplanes are band-limited channels with severe loss beyond 1 GHz, which becomes worse as the channel length increases. This low-pass dispersive channel characteristic obstructs the high-speed data transition and leads to ISI. In order to alleviate this ISI effect, a channel-compensation technique, e.g. equalization, is essential beyond 5 Gbit/sec in legacy FR4 backplane channel longer than 20-in. Meanwhile, as data rate increases, coupling noise becomes another major noise component. Specifically, NEXT noise is dominant factor to deteriorate signal integrity beyond 6 Gbit/sec in the legacy backplane channel. Noise cancellation technique is a promising solution to achieve reliable multi-Gbit/sec transmission in legacy backplane channels.

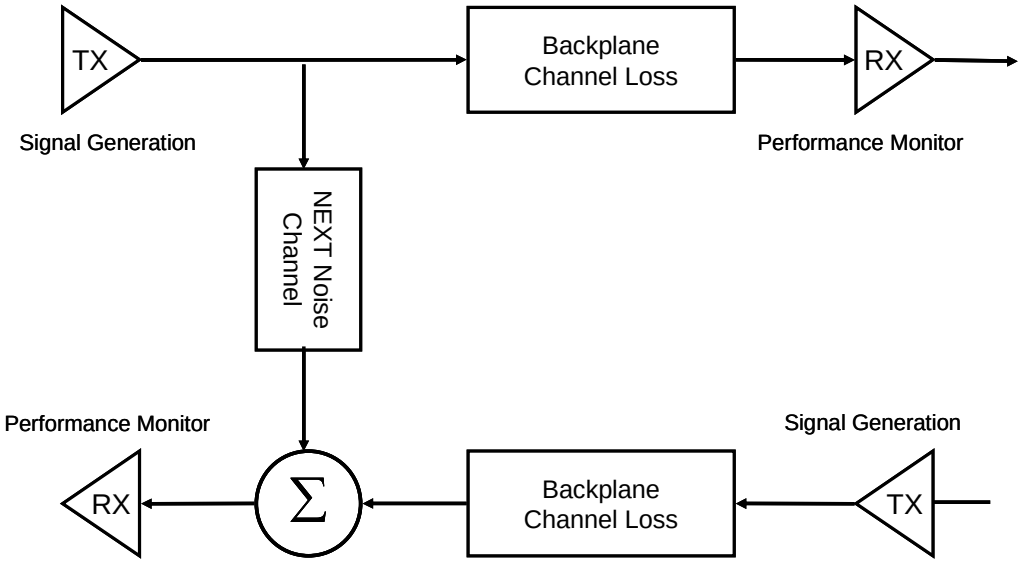


Figure 3.1. Backplane signaling system model

Before implementing the channel-effect mitigation techniques, system simulation is performed to investigate the optimum system solutions and the corresponding building block requirements. Based on the system model, shown in Figure 3.1, the system trade-offs are investigated and the system specification and the functions of building blocks are defined. These resulting specifications are used as the initial design goals in IC implementation.

This chapter provides the historical background of equalization and noise cancellation techniques. Various topologies for the implementation of the signal processing techniques are investigated to derive the optimum system architecture and the corresponding building block specifications. Then, the suggested system architecture is represented, and the system specifications are summarized at the end of this chapter.

3.1. EQUALIZATION

3.1.1. OVERVIEW

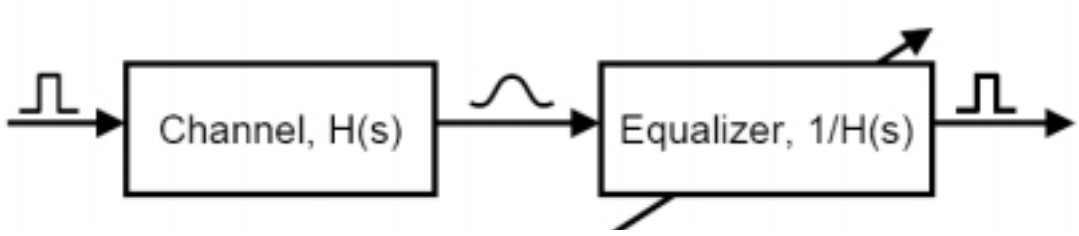
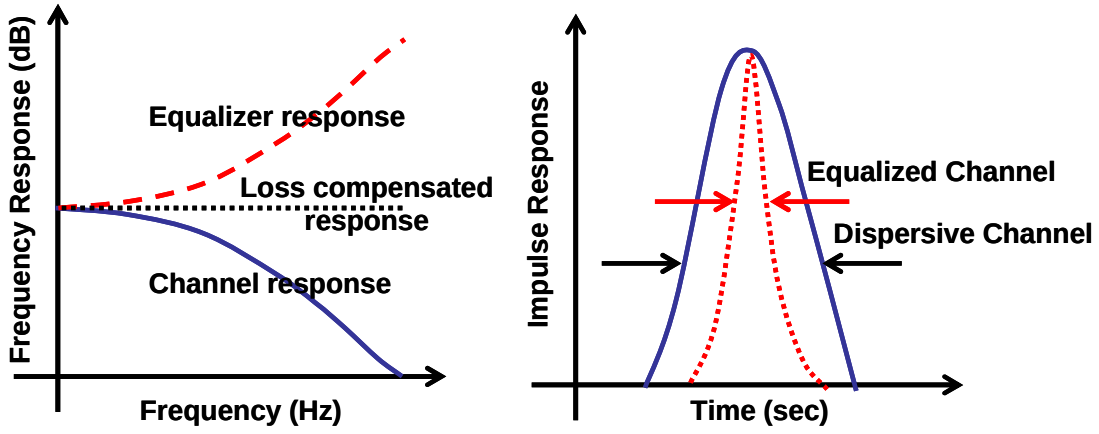


Figure 3.2. System model of equalization for a dispersive channel

An equalization technique compensates the frequency-dependent channel loss characteristics. The band-limited channel has low-pass frequency response, as shown in

Figure 3.3(a). The larger loss in high frequency range causes the signal power to smear into the neighboring symbols. The equalization technique restores the high frequency component of the original transmitted signal. Thus, the frequency response of equalizer has larger gain values for the high frequencies compared to low frequencies around DC, as shown in Figure 3.3(a). Meanwhile, the equalization can be interpreted as a process to sharpen the channel impulse response, as shown in Figure 3.3(b). The width of the channel impulse response means the degree of signal power dispersion in time domain for a given pulse width. Therefore, equalizer can be regarded as a spectrum shaping filter to shorten the channel impulse response to bring it back to its original transmission width. The following sections introduce the historical background and various topologies used in several applications.



(a) (b)

Figure 3.3. Conceptual illustrations of equalization in (a) frequency domain and (b) time domain.

3.1.2. HISTORICAL BACKGROUND

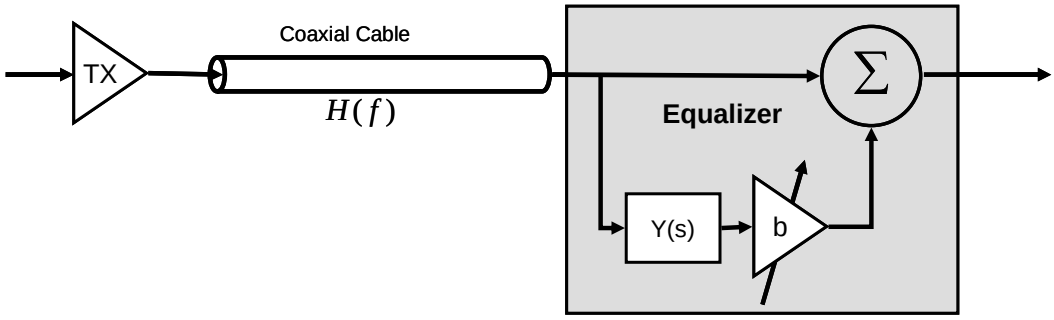
Equalization technique has been widely used to alleviate the ISI effects in several dispersive channels [15-19] such as untwisted pair network cable [16, 17], coaxial cable [15], backplane PCB trace [19], and optical fiber channel [18]. *Shakiba et al.* [15] introduced analog cable equalizer. Coaxial cable channel has attenuation characteristics proportional to the cable length as shown in eq. (3.1). In order to compensate this frequency-dependent channel loss, equalizer transfer function was determined to have the reciprocal of the channel response, i.e. $H^{-1}(f)$, and approximated to the linear superposition of 1 and $b \bullet Y(f)$, as shown in eq. (3.2). The block diagram and frequency responses of the cable equalizer are shown in Figure 3.4 (a) and (b), respectively.

$$H(f) = e^{-aL\sqrt{f}} \qquad \text{eq. (3.1)}$$

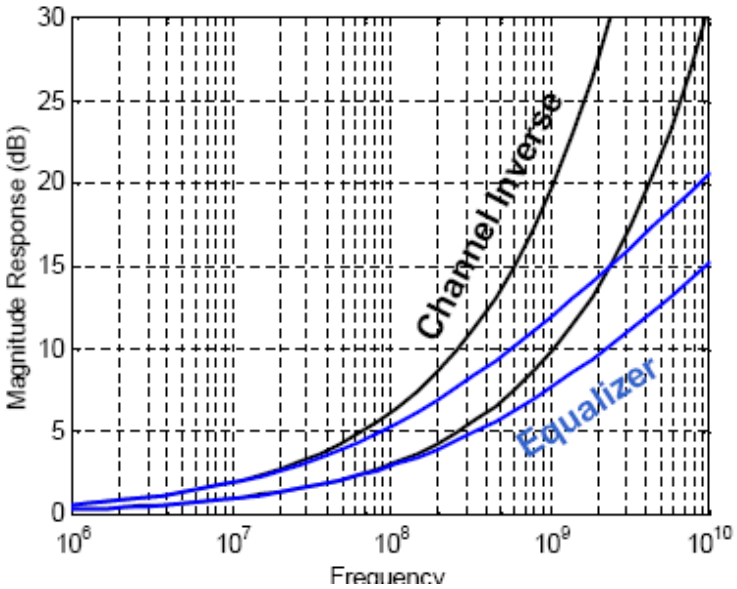
$$H^{-1}(f) = e^{aL\sqrt{f}} \cong 1 + b \bullet Y(f) \qquad \text{eq. (3.2)}$$

The IEEE standard 802.ab 1000BASE-T specified the physical layer for Giga-bit Ethernet (GbE) over CAT-5 cabling system. Since the widely-deployed CAT-5 cabling systems had been used for 100BASE-TX, the 1000BASE-T was supposed to provide smooth way to increase the data rate by ten times over 100BASE-TX. However, CAT-5 cable was not designed to offer enough channel capacity for 250-Mbit/sec data transmission per each cable pair. *He et al.* [16] suggested DSP-based equalizer technique and implemented with a 0.18-um CMOS process technology. This digital equalizer solution had intrinsic problem of power consumption. Thus, *Lee et al.* [17] proposed the mixed-signal IC solution to overcome the power consumption problem of the digital solution. This work adopted sample-and-hold (S/H) based transversal equalizer with

rotating tap weights. The Sign-Sign Least-Mean-Squared-error (SS-LMS) adaptation algorithm was implemented using DACs for the tap weights of the suggested equalizer.



(a)



(b)

Figure 3.4. (a) Block diagram and (b) frequency responses of the coaxial equalizer.

Multimode fiber (MMF) supports multiple modes of light propagation, each with a different velocity resulting in many received pulses of light with different amplitudes, as shown in Figure 3.5. Bandwidth limitations of the receiver front-end smear together pulses into one Gaussian electrical pulse. To address this ISI problem in the MMF

channel, *Wu et al*. [18] implement distribution network by LC ladder type of artificial transmission line, which supported continuous-time signal delay for transversal filter type equalizer. All seven taps with tap coefficient multipliers were used to compensate the Differential Modal Dispersion (DMD) for 10-Gbit/sec NRZ data transmission over 800-m MMF.

Figure 3.5. Signal pulse dispersion due to differential modal dispersion effect of multi-mode fiber channel.

Stonick et al. [19] developed the adaptive transmit pre-emphasis equalizer IC for backplane application. The equalizer IC was implemented with 0.25-um CMOS process technology for 5-Gbit/sec transmission over typical FR4 backplanes. This equalizer pre-distorts the transmission data waveform to combat the channel's dispersive feature. The resulting pre-emphasized waveform was able to compensate the channel loss effect successfully. However, the boosted high-frequency components of the transmitted signal waveform induce the increase of coupling noise between the connector pins. Moreover, as channel loss increases due to longer trace geometry, this technique needs to increase the amount of pre-distortion. Meanwhile, the maximum voltage swing is limited by the system constraints as well as the voltage headroom issue in IC implementation. Thus the resulting decreased average signal level thereby leads to reducing the overall signal-to-

noise ratio. Thus, novel system architecture is still needed to handle the ISI and coupling effects efficiently.

The following sections introduce the background of the various topologies of equalizers widely used in the dispersive channels. Then, the most adequate equalizer topology is selected and optimized for the legacy backplane applications.

3.1.3. EQUALIZER TOPOLOGY STUDY

The basic function of the equalizer is to compensate the channel loss. A simple linear equalizer has the equivalent mathematical transfer function, as shown in eq. (3.3).

$$G_E(f) = \frac{1}{C(f)} = \frac{1}{|C(f)|} e^{-j\theta_c(f)} \qquad \text{eq. (3.3)}$$

,where *C(f)* is the channel characteristic and $G_E(f)$ is equalizer transfer function characteristics [20]. Therefore the amplitude response of the equalizer is $|G_E(f)| = 1/|C(f)|$ and its phase response is $\theta_E(f) = -\theta_c(f)$. As the equalizer transfer function is inverse form of the channel, the equalizer completely eliminates the ISI in theory. This equalizer is called zero-forcing equalizer. For example, the copper channels such as telephone line or twisted-cable have low-pass filter characteristics resulting in increased rising-time and falling-time of the transmitted signal. The increased rising-time and falling-time causes the ISI, in other words, the dispersion in the channel impulse response. The ISI is the main source of the signal distortion in digital communication systems. Figure 3.6 shows the conceptual view of the signal dispersion in lossy channel.

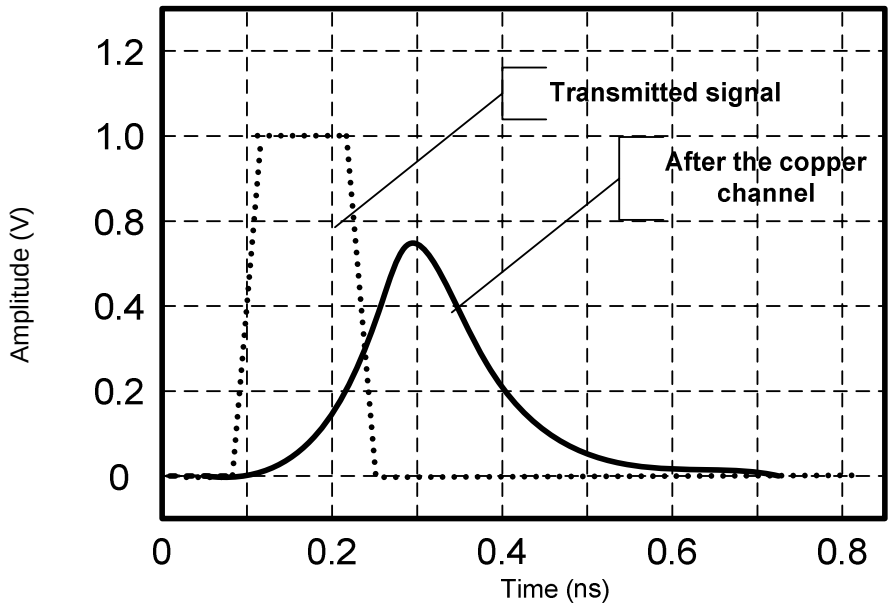


Figure 3.6. Channel impulse response dispersion in copper channel.

Through the equalization at the receiver side, dispersive channel effect can be compensated at the receiver front-end. This work can be done in the receiver side as explained above, or the signal can be transmitted with some intended signal distortion at the transmitter side. This is called pre-emphasis technique. This section will touch the background knowledge of equalization, various types of equalizations, and the pros. and cons. of each equalization technique.

3.1.3.1) Linear equalizer

One of the most common equalizer types is a linear FIR filter with adjustable tap-coefficients, as shown in Figure 3.7. Each tap-coefficient is updated through the certain equalization algorithms. With the FIR structure implementation, there are several equalization algorithm criteria to reduce the ISI.

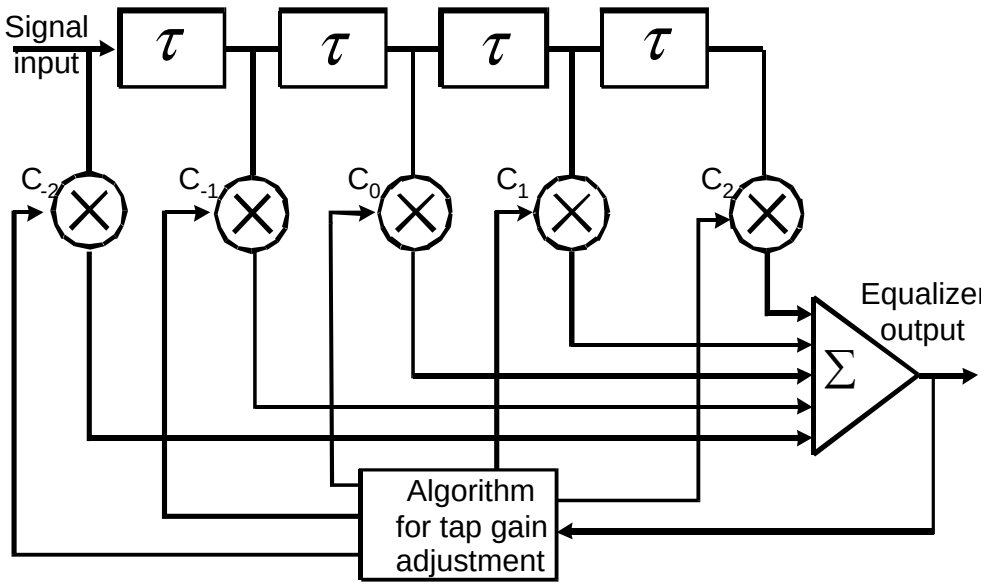


Figure 3.7. Linear FIR equalizer.

Depending on the tap-coefficient extraction algorithms, this linear equalizer is classified to a zero-forcing equalizer and a Minimum-Mean-Squared-Error (MMSE) linear equalizer. The zero-forcing equalizer has the transfer function characteristics as described in eq. (3.3). A time delay element, shown in Figure 3.7, is called tap delay. The tap delay can be as large as symbol interval, and the delayed version of the signal is $x(t-k\tau)$ (where τ=T, T is the symbol period of the signal, and k=1, . . . , n). Also τ can be smaller than T, in this case, it is called fractional tap-spaced equalizer. The fractional tap-spaced equalizer can reduce the aliasing problem in a symbol spaced equalizer and improve the performance assuming the delay is implemented by sampling [21]. As the zero forcing equalizer has inverse channel transfer function characteristic, it can significantly increase the additive noise in the channel. An alternative solution to

ameliorate this problem is the MMSE algorithm, where the tap value is optimized to minimize the power in the residual ISI and the additive noise in the channel.

If the channel frequency-dependent loss characteristics are time-invariant, the channel can be measured and the tap coefficients for the equalization can be extracted from the measured channel characteristics. As the channel is time-invariant, once the tap coefficients are set, the data can be equalized without further adjusting the tap values. However, if the channel is time-variant such as the wireless channel, the equalizer tap values should be updated periodically based on the real-time channel frequency characteristics. The equalizer that can update the tap coefficient by tacking the channel characteristics is called an adaptive equalizer. Most commonly used adaptive equalization algorithm is Least-Mean-Squared (LMS) error algorithm [22]. The tap coefficients updated by the LMS algorithm are shown in eq. (3.4).

$$p(k+1)=p(k)-\mu\frac{\partial E[e^2]}{\partial p} \quad or \quad p(k+1)=p(k)+2\mu\cdot e(k)\cdot\phi(k) \qquad \text{eq (3.4)}$$

, where p(k) is the tap coefficients, μ is the parameter controlling the adaptation rate, $e(k)$ is the error signal between the desired signal and received signal, and $\phi(k)$ is the derivative form of the received signal (i.e. $\partial y/\partial p$, where y is the signal after the adaptive equalization). Figure 3.8 shows the one example of adaptive equalization. In this example, the transmitted signal is required at the receiver side (i.e. training sequence) as shown in Figure 3.8 (a), or desired signal can be extracted from the receiver's decision block as shown in Figure 3.8 (b).

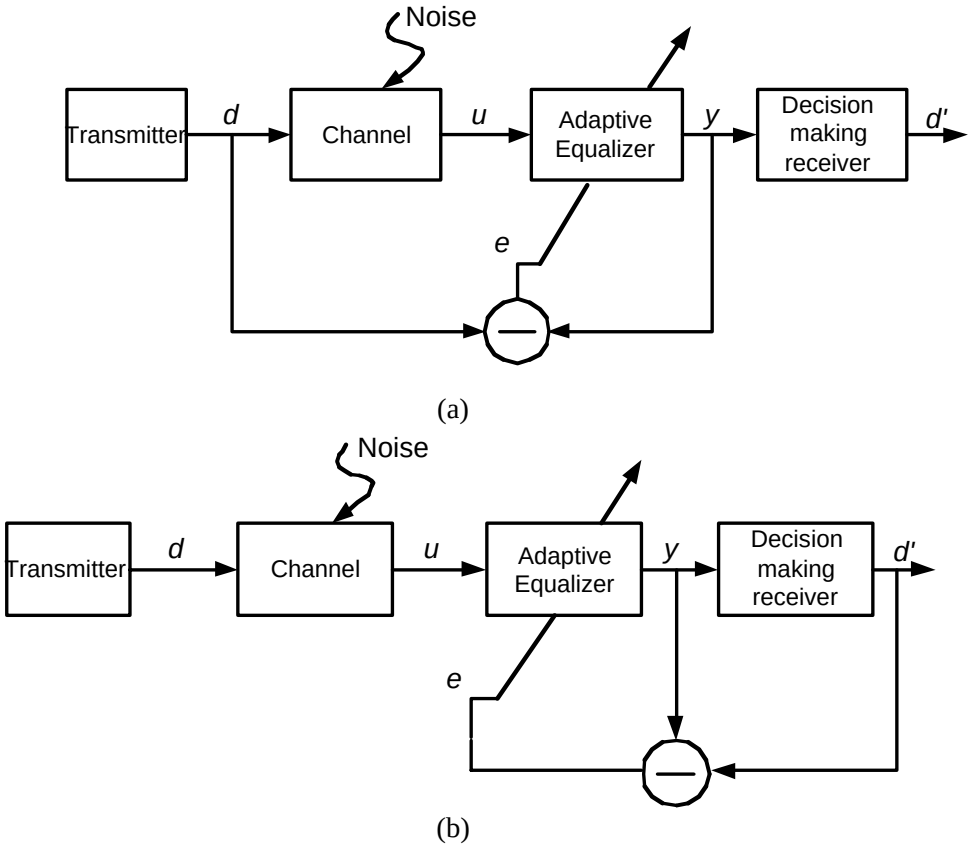


Figure 3.8. Adaptive equalization (a) using training sequence and (b) using the decision signal at the receiver as the desired signal.

The practical implementation of the LMS algorithm induces hardware complexity. So there are several alternative simplified algorithms to reduce the burden in hardware implementation. The simplified version of LMS algorithms is shown in eq. (3.5-7) [23].

Sign-data LMS: $p(k+1)=p(k)+2\mu \cdot e(k) \cdot sgn(\phi(k))$ eq. (3.5)

Sign-error LMS: $p(k+1)=p(k)+2\mu \cdot sgn(e(k)) \cdot \phi(k)$ eq. (3.6)

Sign-sign LMS: $p(k+1)=p(k)+2\mu \cdot sgn(e(k)) \cdot sgn(\phi(k))$ eq. (3.7)

Even though the advantage in hardware implementation, these simplified algorithms may not converge or may have more iterations than the original algorithm.

3.1.3.2) Nonlinear equalizers

Linear equalizers described in previous section are very effective on channels such as wire line and telephone line channels, where the ISI is not so severe. However, in some channel environments having spectrum nulls, the linear equalizer will introduce large amount of gain to compensate the spectrum null. Thus, the noise in the channel will be enhanced severely. Such channels are often encountered in mobile radio channel, such as those used for cellular radio communications.

A Decision Feedback Equalizer (DFE) is a nonlinear equalizer that employs previous decisions to eliminate the ISI caused by the previously detected symbols on the current symbol to be detected. The block diagram for the DFE is shown in Figure 3.9. The DFE is typically used with the conjunction of linear FFE. Even though the linear FFE alone can be used to cancel the ISI, the combination of the linear FFE and DFE has better performance. The principal reason for this improvement is that the DFE uses the linear combination of the noiseless binary decisions to eliminate some of the ISI and does not add noise at the input of the decision circuit. The linear FFE amplifies the high-frequency portion of the signal and the noise to cancel the ISI, which is not compensated by DFE. So the noise enhancement of the linear FFE in conjunction with DFE is less than the one when the linear FFE alone is used. Recently, the DFE is reported as a good candidate for backplane channel equalization, where the NEXT noise is severe [24]. Otherwise, the FFE alone will significantly amplify the NEXT noise because the NEXT noise channel frequency response is similar to the high-pass filter response. One potential problem with a DFE is the error propagation [23]. If the DFE provides an incorrect decision, the error will propagate through the feedback filter and increase the probability that another incorrect decision will be made.

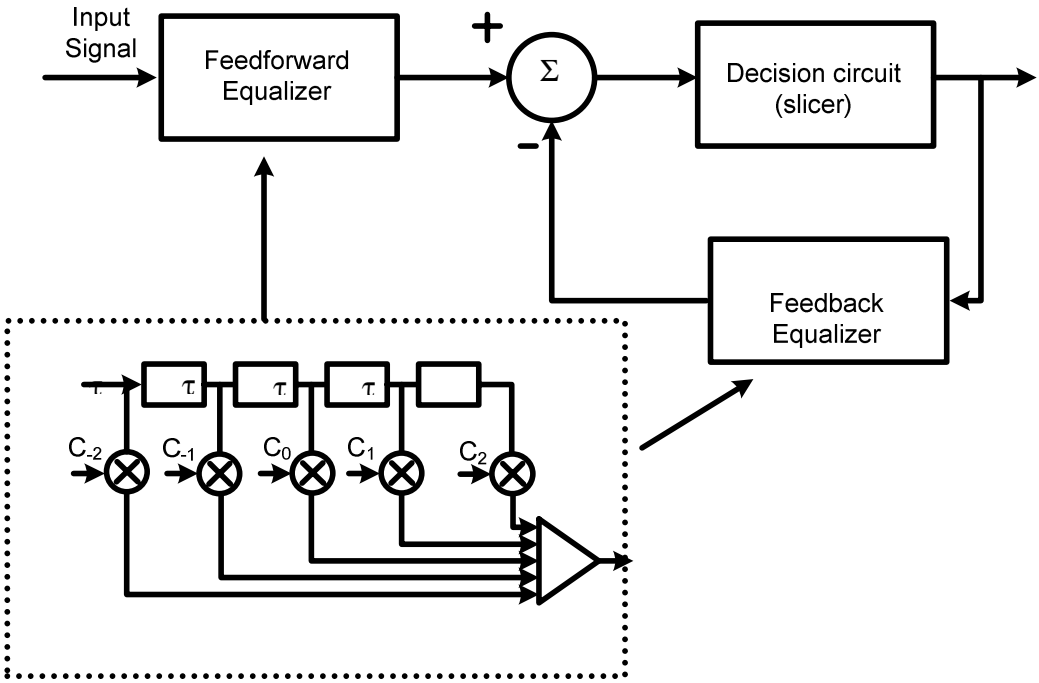


Figure 3.9. Block diagram of the DFE.

Consequently, there was suggested another algorithm, which finds the sequence that maximizes the joint probability of the received sequence conditioned on desired sequence. This sequence is called the maximum-likelihood sequence detector. An algorithm that realizes maximum-likelihood sequence detection (MLSD) is the Viterbi algorithm. Partial-response maximum-likelihood (PRML) detectors using various implementations of the Viterbi algorithms have been widely adopted for hard disk drive read channel [25, 26]. Meanwhile, the major drawback of MLSD is the exponential behavior of the computational complexity, which is a function of the ISI span. Thus the MLSD is practical for the channel where the ISI spans only a few symbols [20].

3.1.3.3) Cable equalizer (Bode equalizer)

In this section, one typical form of the equalizer specifically for the cable channel will be covered. As the cable channel can be modeled with simple low-pass filter transfer function, the cable equalizer can be implemented with the combination of the high-pass filter with several poles as design parameters and variable gain controller as shown in Figure 3.10.

The variable gain can be controlled via a LMS or other algorithm for adaptation. The cable equalizer is practical solution to implement by analog continuous-time signal processing. The continuous-time equalization techniques have some advantages over discrete-time solutions. For example, the continuous-time equalizer does not need any sampling-phase recovery block, so that the equalizer adaptation can be realized independently with the timing recovery function [15]. Also the continuous-time equalization is well fit for high-speed operation over the discrete-time counterpart as it does not need any high-speed sampling function. Despite these advantages, the cable equalizer has some potential problem that it can boost up the high-frequency noise, which is the similar phenomenon in the linear FFE.

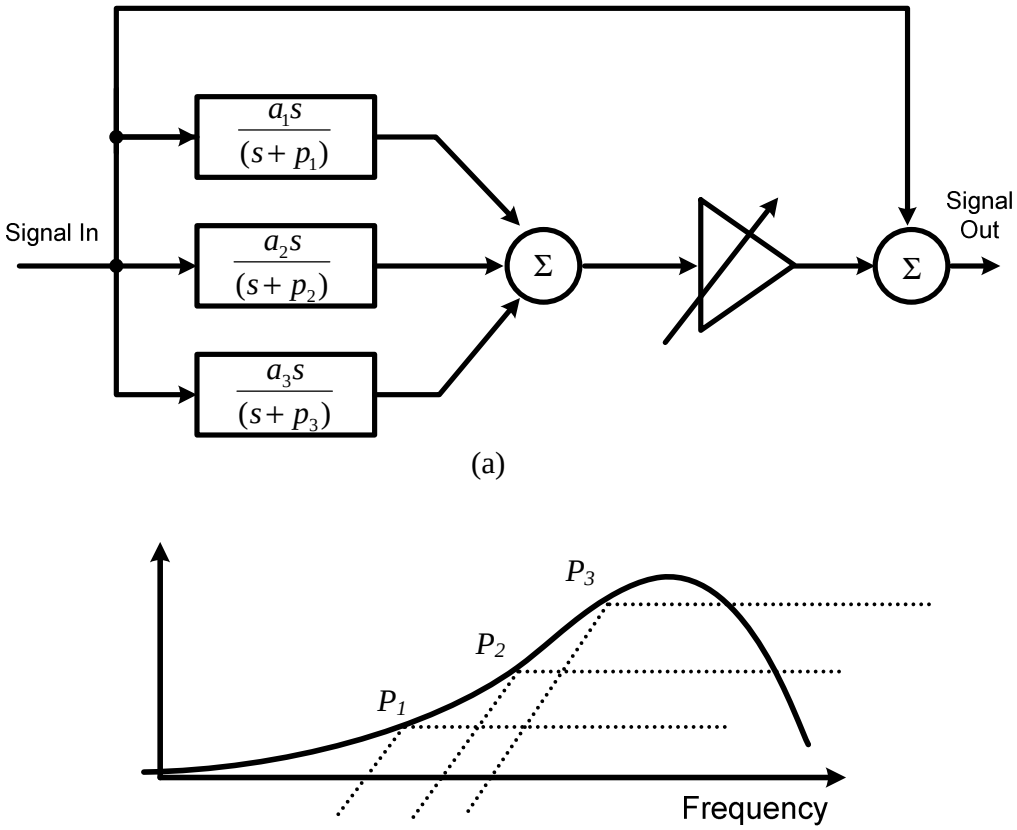


Figure 3.10. (a) Block diagram for the simple cable equalizer. (b) the corresponding equalizer frequency response

3.1.3.4) Transmitter- and receiver-side equalizer

As it is mentioned previously, the equalizer can be installed at the transmitter side or receiver side. The conceptual block diagram is shown in Figure 3.11. The transmitter-side equalizer, which is called pre-emphasis, is easily implemented by FIR filter type with digital control. However, the pre-emphasis technique boosts up the high-frequency portion on the transmitter side increasing the NEXT noise for high-speed chip-to-chip interconnections. Additionally, the pre-emphasis requires the information sent from the receiver side for dynamic or fine-tuned tap-coefficients updates. Furthermore, as channel

loss increases, the pre-emphasis needs to apply more gain to boost the high frequency components of the transmit signal. Since the maximum signal swing is limited by the system constraints and the IC process technology, the average signal swing level at the transmitter side needs to be decreased thereby requiring additional gain at the receiver side. By these reasons, the equalizer at the receiver side is better candidate over the pre-emphasis for adaptive or fine tuned equalization. However, as it is mentioned previously, the FIR type equalizer alone at the receiver side enhances the noise at high frequency ranges, while it compensates the channel loss to reduce the ISI.

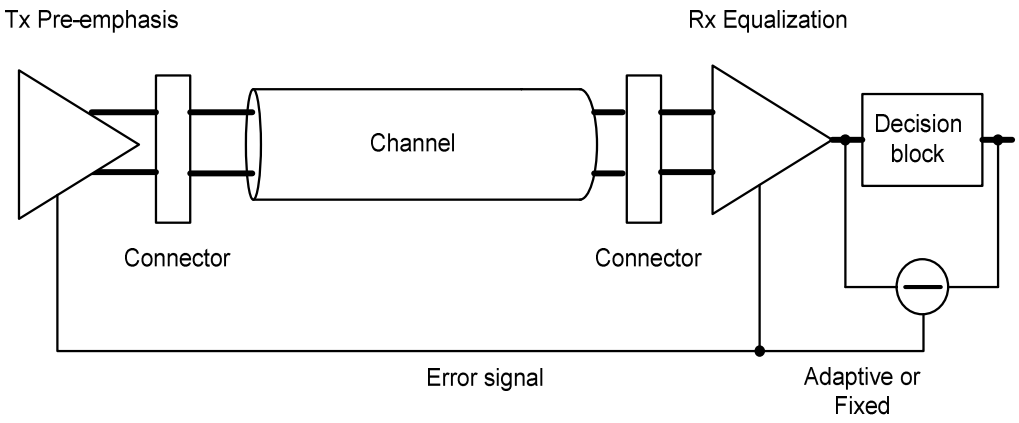


Figure 3.11. Equalization at the transmitter side, receiver side and both side.

It is also possible to use the combination of the pre-emphasis and receiver-side equalization to further increase the overall bit error rate (BER) of the high-speed interconnections. The resulting gain-boosting requirement for specific spectral loss can be relaxed for each equalizer. However it needs more complex hardware implementation increasing the overall system cost.

For the digital communication systems, the equalizers have been implemented with digital circuitry below Gbit/sec. For example, the wireless communication system requires the equalization to compensate the multi-path fading effects. However, as the data rate is increased over multi-Gbit/sec, the conventional digital approaches are not proper solution anymore. By this reason, several I/O standards such as XAUI, PCI-express, and UXPI have been emerged to address any high-speed interconnection problems in system- and packaging-level. Moreover, in an IC implementation point of view, there have been several efforts to implement the equalizer by the continuous-time analog signal processing, the mixed-signal circuit, or the RF/microwave techniques over conventional digital circuit approaches [18, 27, 28].

3.1.4. EQUALIZER SYSTEM SIMULATION

Backplane channel has coupling noise effects from the connector pins. This coupling effect must be considered to select the optimum equalizer architecture for the backplane channel. In order to select the optimum equalizer type, transmit-side and receiver-side equalizers are examined for the backplane channel environment. Then, the equalizer architecture and the corresponding signal processing algorithm are investigated for optimum performance.

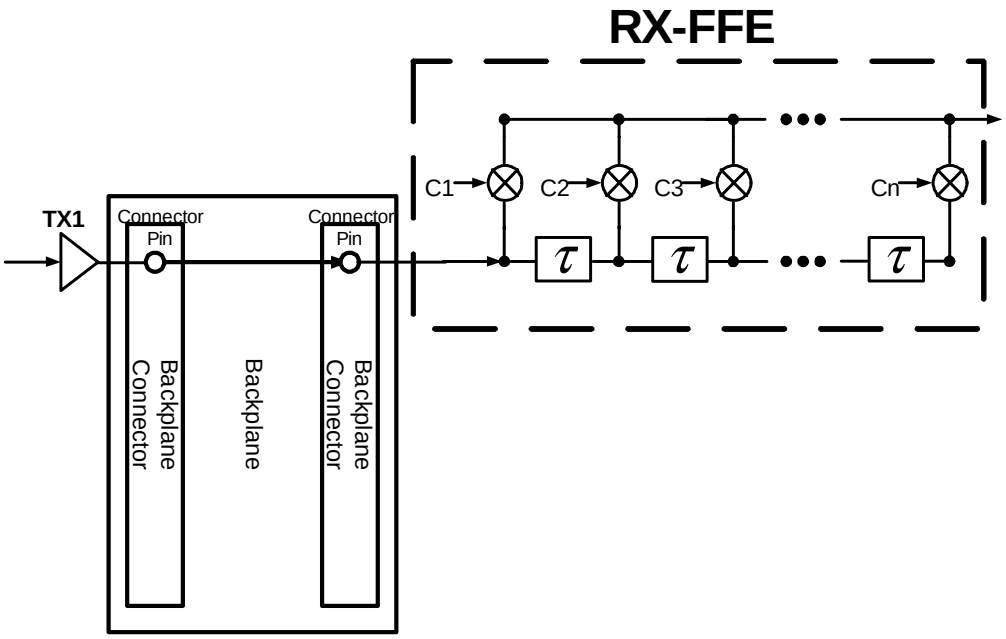


Figure 3.12. Block diagram of receiver FFE with FIR filter structure.

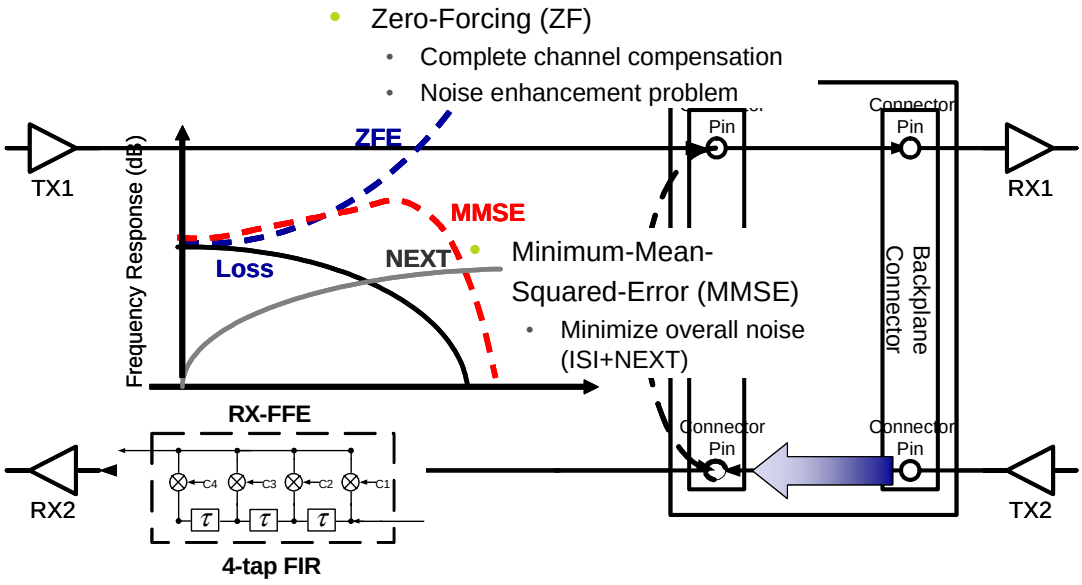


Figure 3.13. Transfer function of the ZF-LE and the MMSE-LE for 20-in FR-4 backplane channel.

A transmit equalizer pre-emphasizes the transmit signal waveform to combat ISI [19]. As channel loss increases, this transmit equalizer needs to apply more pre-emphasis to boost the high frequency components of the transmit signal. Since the maximum voltage swing is limited by system constraints and the CMOS voltage headroom, the average signal level needs to be decreased thereby requiring additional gain at the receiver. Moreover, the transmit equalizer uses channel information fed back from the receiver to adjust the tap gains for compensating the channel loss. This means that the transmit equalizer has to be controlled by both the transmitter and the receiver. Meanwhile, a receiver equalizer does not change the transmit signal level. Therefore, the receiver does not need the additional gain that is required in the transmit equalizer scheme. The receive side equalizer is simply adjusted using the channel information obtained by an eye-monitoring unit [28] at the receiver. Additionally, this channel information is reused by NEXT noise canceller. As a result, the receiver equalizer integrated with a NEXT noise canceller can be configured in a more efficient way than a transmit equalizer.

A receiver-side FFE is implemented using a FIR filter structure. The FIR filter consists of variable gain amplifiers for tap gains and a Tapped Delay Line (TDL), as shown in Figure 3.12. These tap coefficients are derived from the measured impulse response data set. Equalizer tap coefficient values are calculated based on the measured backplane channel impulse responses using signal processing algorithms such as Zero Forcing-Linear Equalizer (ZF-LE) and Minimum-Mean Squared-Error-Linear Equalizer (MMSE-LE) [20]. As the transfer function of ZF-LE is the reciprocal of the channel transfer function, it can remove ISI completely but does so neglecting the impact of high-frequency crosstalk, which is also amplified. In contrast, MMSE-LE can ameliorate this

noise enhancement problem, since its tap coefficients are calculated to minimize overall signal degradation from both ISI and crosstalk noise. Figure 3.13 shows the frequency response for the ZF-LE and MMSE-LE solution to a 20-in FR-4 backplane channel.

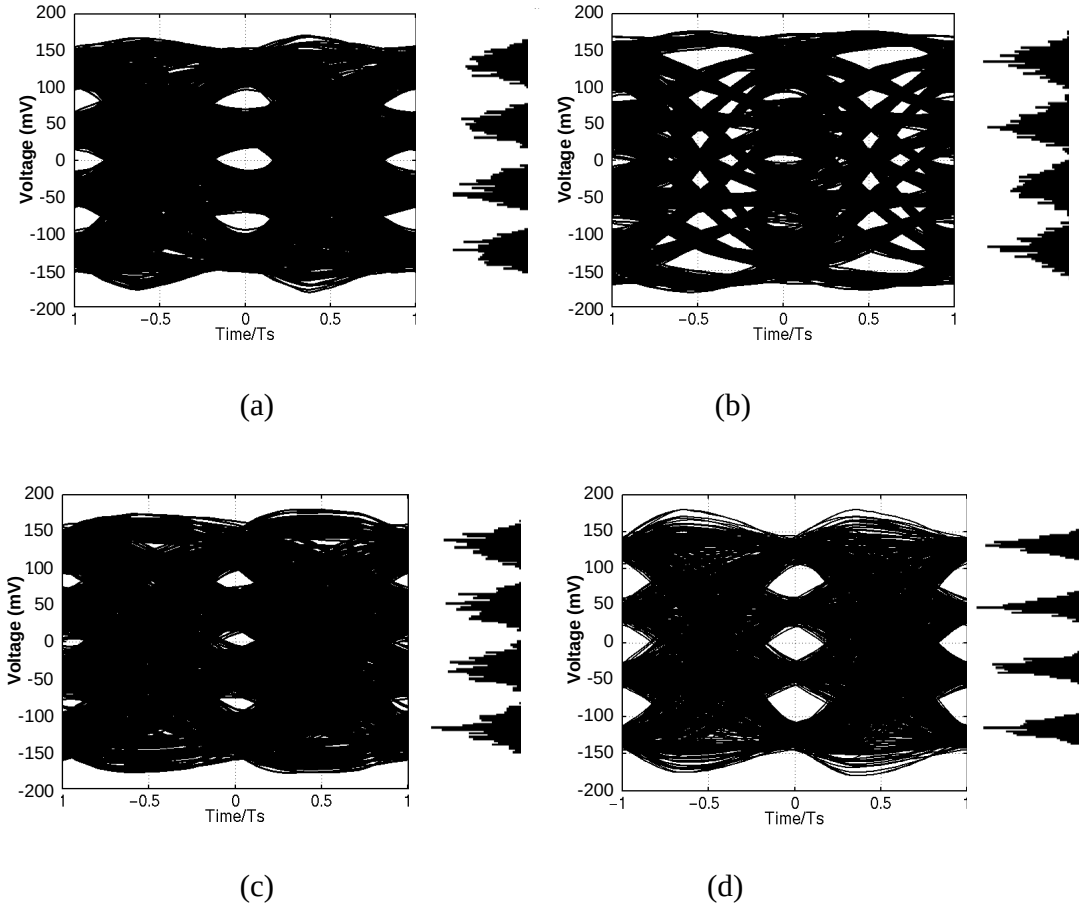


Figure 3.14. Eye diagrams for the proposed FFE output. (a) 3-tap Ts/2-spaced FFE, (b) 4-tap Ts/2-spaced FFE, (c) 3-tap Ts/3-spaced FFE, and (d) 4-tap Ts/3-spaced FFE.

In order to obtain the optimum FFE configuration and values of the tap coefficients, the performances of the equalizer with different tap-spacings and number of taps were simulated. Figure 3.14 shows the eye diagrams and histogram plots of Ts/2 and Ts/3-spaced FFE output signals for 3- and 4-taps respectively, without an aggressor source,

where Ts is the symbol duration (i.e. 100 ps) of 20-Gbit/sec 4-PAM signal. The Ts/3-spaced 4-tap equalizer has the largest voltage margin and eye-opening size compared to other configurations, as shown in Figure 3.14 (d).

In this section, the Ts/3-spaced, 4-tap receiver-side FFE was determined as the optimum equalizer structure. The optimum tap coefficient values were calculated with the MMSE algorithm. The corresponding building blocks are tap delay line with 33-ps tap-spacing and variable gain block with bi-polar gain value within -1 ~ +1. These basic definitions and specifications of the building block functions will be used to design and implement the corresponding building block ICs. The details of the IC implementation are introduced in the chapter 4.

3.2. NEXT NOISE CANCELLATION

3.2.1. OVERVIEW

The NEXT noise is major signal integrity impairment factor, as mentioned in the chapter 2. In order to address this NEXT noise effect, there have been developed the advanced connectors with the improved coupling characteristics [9, 10]. Meanwhile, these sophisticated connectors are being deployed just to the upgraded backplane systems, but not to legacy backplane systems considered herein.

Due to the dramatic advances of silicon IC technology, noise cancellation techniques have been realized for various applications [5, 6] and their performances were proven. This add-on IC solution doesn't need replacing the connectors or any physical configuration of data interface infrastructures. Thus, this noise cancellation approach has

been considered cost-effective and versatile solution to be adjusted to diverse channel environments.

Figure 3.15 introduces the backplane signaling environment affected by the NEXT noise coupling phenomenon. The high speed transceivers are mounted on line cards. These line cards are plugged into the backplane board through the connectors. Multi-Gbit/sec data streams are transferred through the transmission lines as well as the connectors. These signals experience the channel loss from the backplane and the line card PCB boards. Thus, the resulting signal amplitudes are attenuated and waveform edges are smoothened. In the meantime, the transmit signal is coupled to the adjacent channel's received signal through the coupling channel between the connector pins.

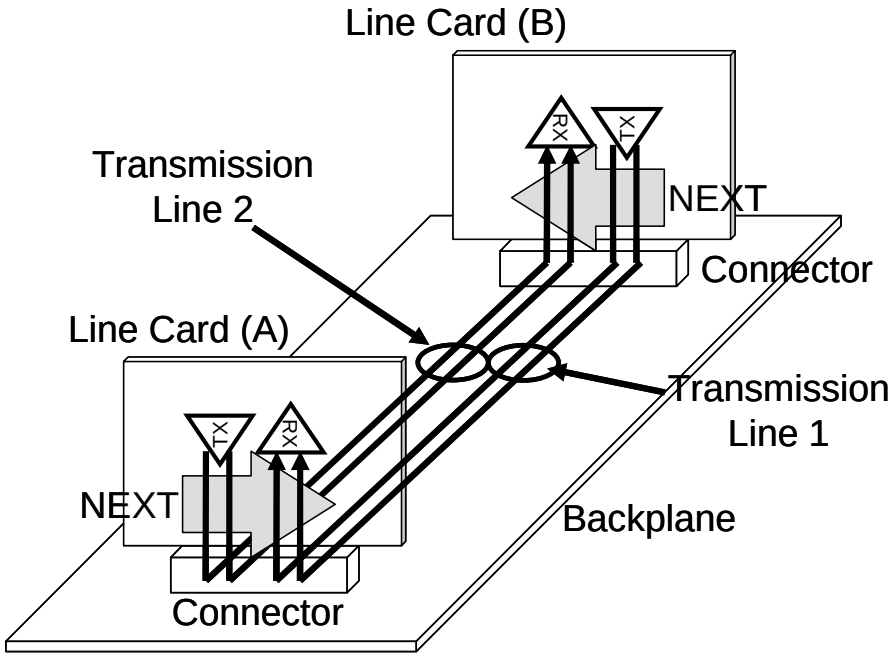


Figure 3.15. Backplane signaling environment affected by the NEXT noise coupling phenomenon.

In general, this NEXT noise channel has high-pass frequency response. The corresponding noise waveform has peaks at each data transition of aggressor signal, i.e. the neighboring transmit signal. In other words, the NEXT noise is data-dependent noise coming from the known noise source through the NEXT coupling channel, as shown in Figure 3.16.

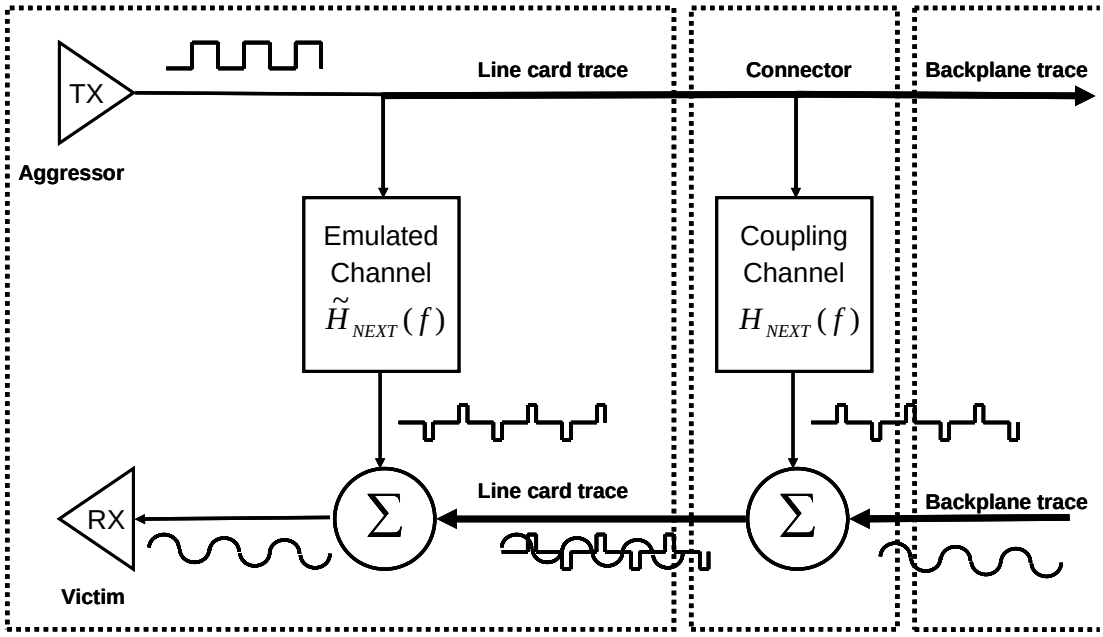


Figure 3.16. System model of backplane NEXT noise cancellation.

If this NEXT noise is generated by mimicking the actual NEXT channel $H_{NEXT}(f)$, this emulated noise can be cancelled out with the original coupled noise. This is the fundamental operation of NEXT noise cancellation. The coupling noise is emulated by filtering the aggressor signal with NEXT channel emulating filter $\tilde{H}_{NEXT}(f)$. This emulated noise waveform has opposite polarity to the original noise waveform to be cancelled out. Meanwhile, these two noise signals go through different physical signal

paths. The emulated noise has small delay by passing through the channel emulation filter. However, the original NEXT noise has additional delay induced by the line card traces and connector pins. This delay difference must be compensated by applying delay adjustment to the emulated noise waveform.

The following section introduces the historical background of noise cancellation technique. Then, the system simulation provides the optimum architecture and specifications of the building blocks.

3.2.2. HISTORICAL BACKGROUND

Noise cancellation techniques have been widely used to alleviate echo noise and crosstalk noise effects in various applications [5, 6, 29-31] such as the xDSL, the GbE, optical storage, chip-to-chip interface, and backplane application. The noise cancellation techniques adopted in each application are introduced in the following sections.

3.2.2.1) xDSL-crosstalk noise cancellation

Digital subscriber line (DSL) technology exploits the existing copper plant to transfer data at Mbit/sec rates for high-speed internet and other digital transmission services. In this technology, the DSL signal travels on a twisted-pair loop from the central office to the subscriber. Many, sometimes thousands, twisted-pairs are bundled together in a single cable. Telephone loops were designed and built to carry voice services, and at these frequencies crosstalk is insignificant. However, at higher frequencies crosstalk becomes major impairment. Considering the bundle as a multi-input/multi-output channel, the NEXT signals for a particular line can be cancelled by using an adaptive filter for each adjacent transmitted signal. This method can be very expensive if the bundle has a large

number of twisted pairs. *Nongpiur et al.* [29] proposed a crosstalk noise cancellation technique comprising of the crosstalk-detecting means and adaptive filter to cancel each of crosstalk sources detected. By taking cross-correlation of the adjacent transmitted signals with the received signal, the crosstalk signals were detected and then cancelled by the channel emulating digital adaptive filter. This technique was implemented with digital solutions having intrinsic problem of power-consumption, speed limitation, and hardware complexity.

3.2.2.2) Gigabit Ethernet – echo noise cancellation

The Gigabit Ethernet on copper cable is a fast evolving technology enabling 1-Gbit/sec full-duplex data communication over the existing UTP CAT-5 cables. As depicted in Figure 3.17, four pairs of twisted-pair cables and eight transceivers (four at each end) with 250-Mbit/sec data rate offer 1-Gbit/sec data communication. Five-level pulse amplitude modulation (5-PAM) reduces the baud rate to 125 MHz. In full-duplex communication, a hybrid is typically used to isolate the receiver from the transmitted signal. However, cable and connector impedance variation still results in substantial leakage of the large transmitted signal, thereby creating near-end echo. Also, the impedance discontinuity along and at the end of the cable produces the far-end echo. In addition, the NEXT between the four cables is significant.

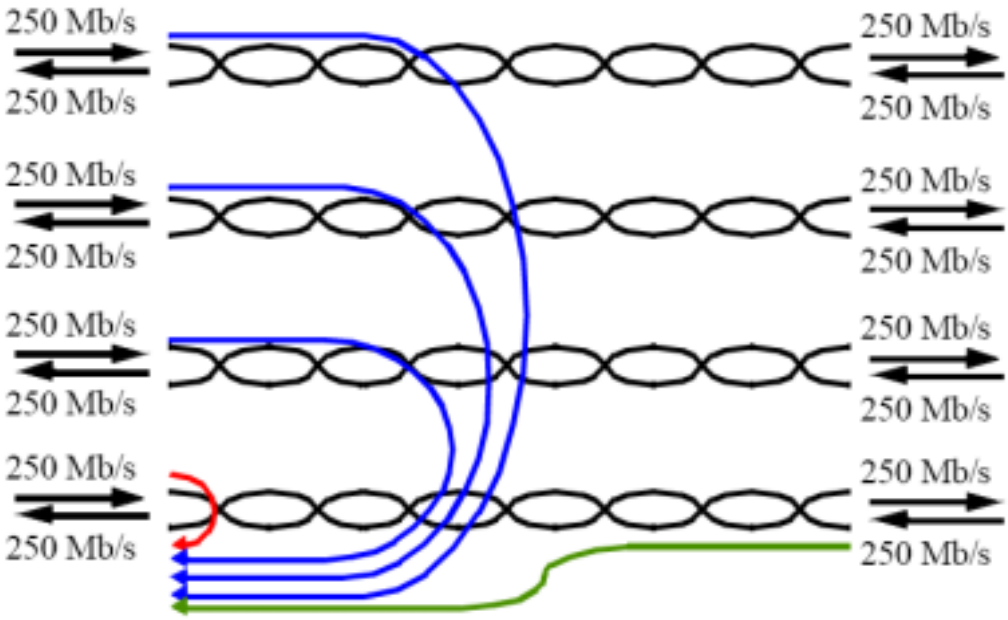


Figure 3.17. The IEEE standard 802.ab 1000BASE-T over CAT-5 cabling system

Lee et al. [30] proposed a mixed-signal echo canceller to partially cancel the echo in the analog front-end, relaxing the complexity in the digital domain. Using a LMS algorithm, the circuit adapts the four taps of a discrete-time analog FIR filter at the startup, thus canceling the four largest echo signals between two transceivers. The IC was fabricated in a 0.4-um CMOS technology, and the resulting circuit reduced the echo power by 10 dB at 125 MHz.

3.2.2.3) Optical storage – crosstalk cancellation

As multi-media data content requires high-fidelity, the data file size increases dramatically. Although compressed, the signal requires broader bandwidth and higher storage capacity than usual; in other words, handling HDTV means dealing with high density optical recording. Given the optics, i.e. the diameter of the laser light spot, to achieve a high information density in the radial and tangential directions one must

increase the number of data bits that can be resolved per spot. Then, one must increase the linear density, namely the number of bits per unit length along a given track, and reduce the track pitch, the distance between adjacent tracks. Interference between tracks becomes significant because a greater amount of light impinges on neighboring tracks, and the detector picks up unwanted signals.

Bellini et al. [31] suggested a crosstalk cancellation technique for the compact disk optical storage application. The multi-spot detection system was developed and made use of three spots; the central spot lights the useful track, while the adjacent ones are focused on the two neighboring ones. The three signals are the impulse responses of the useful and adjacent channels. The suggested technique made it possible to estimate the interference of adjacent tracks, and clean up the useful signals.

3.2.2.4) Parallel bus interface – crosstalk cancellation

With continued scaling of device features and interconnect dimensions down to deep-sub-micron and nanometer range, interconnects are becoming the limiting factor for performance and reliability in many system-on-chip (SoC) designs. Since the overall chip dimensions continue to increase with increasing system complexity, interconnects - especially the long-distance connections between various system blocks on chip - tend to get longer. At the same time, wire width and wire separation continue to drop while their cross-sectional area is scaled down at a slower rate to prevent resistance values increase dramatically. This ongoing trend of controlling the RC delay, combined with the faster rise/fall times and longer wires, makes the inductive part of the wire impedance become comparable to its resistive part. Thus, inductive effects, and more specifically, mutual inductive coupling between neighboring wires, become non-negligible in recent very

deep sub-micron technologies.

Zerbe et al. [6] implemented a crosstalk noise cancellation technique for the multi-drop bus interface system in chip-to-chip data interface application. The developed IC reduced the coupling noise effects from adjacent on-chip signal lines. The aggressor signal is tapped off and amplified by the multiplier with variable gain, as shown in Figure 3.18. This emulated noise is added to the transmit signal and cancelled at the multi-drop bus interface. In this work, the coupling characteristic was assumed simple enough to be emulated with a single amplifier. Thus, this technique can not be applied to the backplane NEXT channel having complicated frequency response.

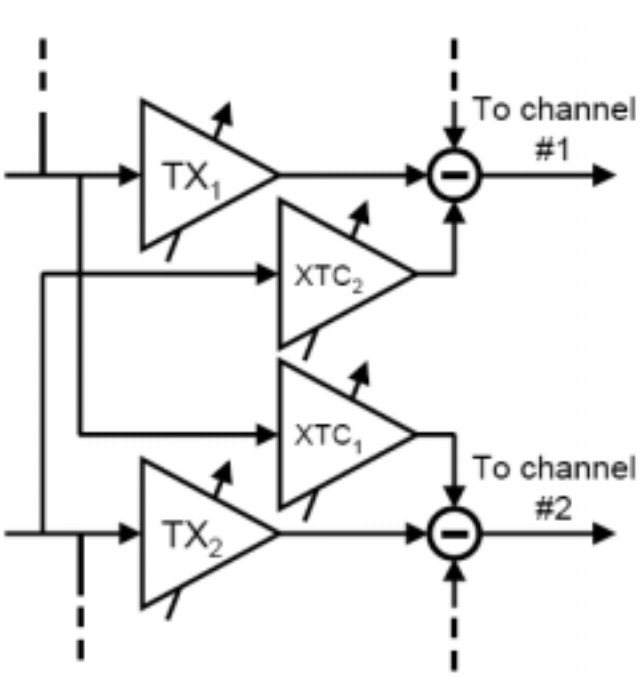


Figure 3.18. Crosstalk noise cancellation technique for chip-to-chip data interface

3.2.2.5) Backplane – crosstalk cancellation

Bien et al. [5] introduced a backplane NEXT noise cancellation IC at 6.25 Gbit/sec fabricated in a standard 0.18-um CMOS process. In this work, a 5-tap FIR filter was adopted to emulate the NEXT channel characteristic having high-pass frequency response, as shown in Figure 3.19. This 5-tap FIR filter was designed to mimic the NEXT channel frequency response and showed close match with actual noise characteristics up to 6 GHz. Meanwhile, since the NEXT frequency response has peak around 6 GHz and then starts decreasing, emulating the NEXT channel frequency response becomes more challenging beyond 6 GHz. Thus, this 5-tap FIR filter is not enough to emulate the NEXT channel for higher data rate transmission above 6 Gbit/sec. In other words, 10-Gbit/sec (and beyond) application needs a novel system architecture for NEXT noise cancellation to improve the cancellation performance.

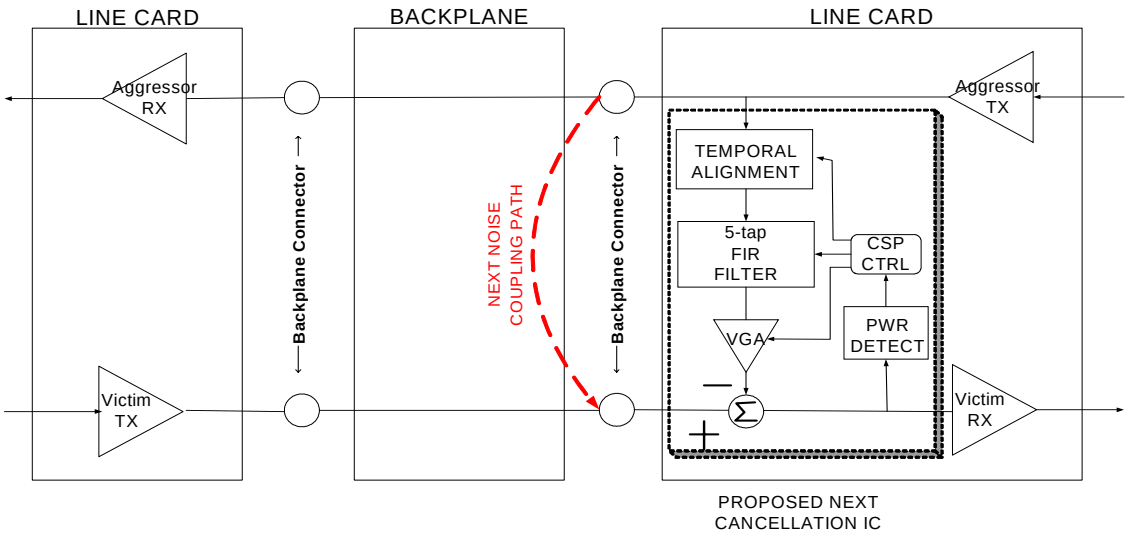


Figure 3.19. System architecture for the NEXT noise cancellation IC suggested in [5].

3.2.3. NEXT CANCELLATION SYSTEM SIMULATION

This section suggests the system architecture for 4-PAM, 20-Gbit/sec data transmission over legacy backplane channel. System simulations are performed to investigate the system requirements of building blocks. Then, NEXT noise cancellation performance is simulated.

Generally, the NEXT channel has high-pass frequency response as shown in Figure 2.9. However, this response depends on the connector type and has the peak values at different corner frequency values, i.e. 3, 4, 5 GHz for connector type A, B, and C, respectively. As data rate increases, the corresponding signal bandwidth is also increasing. As a result, NEXT channel response beyond this corner frequency affects the signal integrity. This requires more accurate NEXT channel emulation close to actual channel for the frequency beyond the corner frequency of the channel response. In order to improve this channel emulation accuracy, this work suggests a system architecture having dual stage of NEXT noise cancellation, i.e. coarse and fine noise cancellation. These two stages employ two filters to emulate the NEXT channel response as shown in Figure 3.20. A tunable Pole-Zero (PZ) filter approximates the NEXT channel response below the corner frequency and generates the emulated NEXT noise for the coarse cancellation procedure. Once the coupled NEXT noise is cancelled out by coarse channel emulation filter, a 7-tap FIR mimics the NEXT channel response beyond the corner frequency to remove the residual NEXT noise after the coarse cancellation. As mentioned in the section 3.2.1, the original coupled and emulated NEXT noise waveforms have delay difference. A temporal delay alignment block compensates this delay difference by applying additional propagation delay to the emulated noise source.

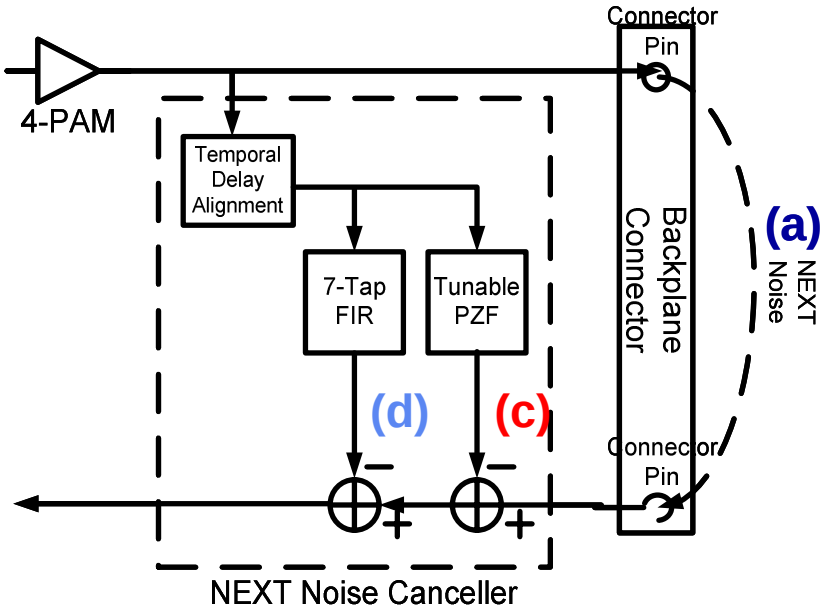


Figure 3.20. System architecture of suggested NEXT noise cancellation technique.

Figure 3.21 shows the frequency response of the actual backplane NEXT channel and the simulation results of the NEXT channel emulation filters. The PZ filter response (c) emulates the actual channel response below the corner frequency 5 GHz. The resulting coarse emulated noise is cancels out the dominant power of the NEXT noise. In order to remove the residual noise, the FIR filter response (d) mimics the channel response beyond 5 GHz. Through the system simulation, the 7-tap FIR filter with 33-ps tap spacing was adopted for the fine cancellation of the residual noise. The resulting overall channel emulating frequency response (b) with the PZ filter and the FIR filter show close match with the actual NEXT channel response (c).

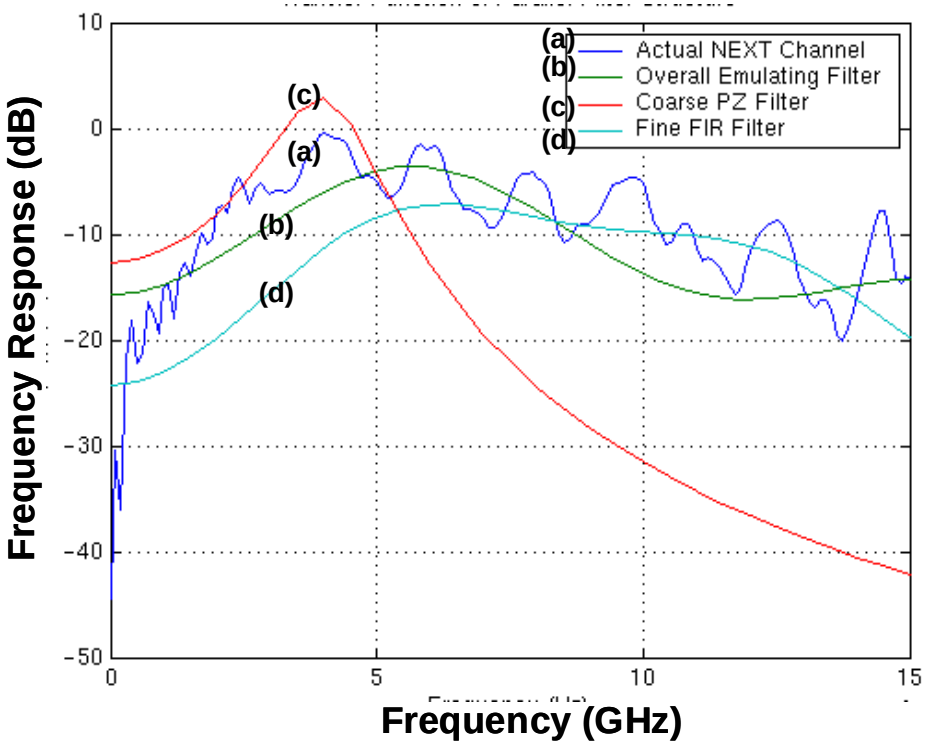


Figure 3.21. Frequency response of the actual backplane NEXT channel and the simulation results of the NEXT channel emulation filters.

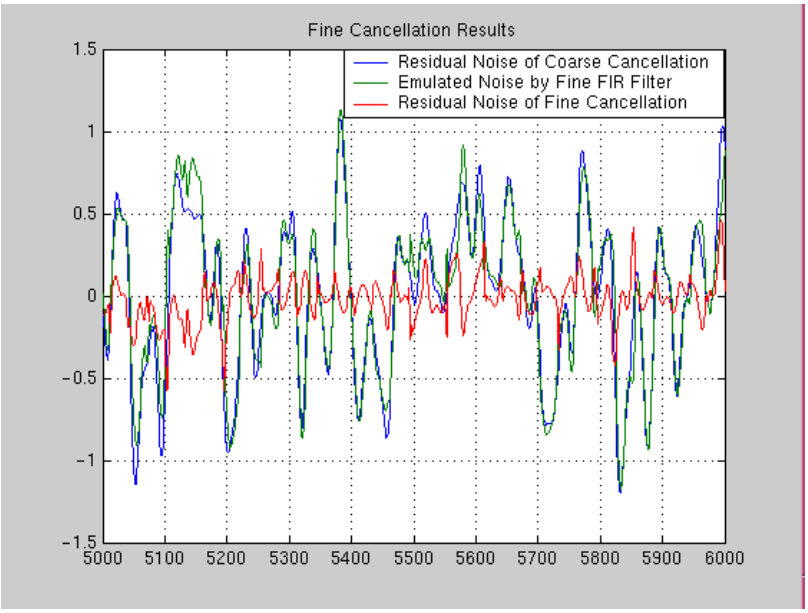


Figure 3.22. The simulation results of the fine noise cancellation procedure

Figure 3.22 shows the results of the fine noise cancellation procedure. The noise waveform emulated with the fine channel emulation filter is quite well matched with the residual noise waveform of the coarse cancellation. The resulting remained noise after this fine cancellation has half of the residual noise power.

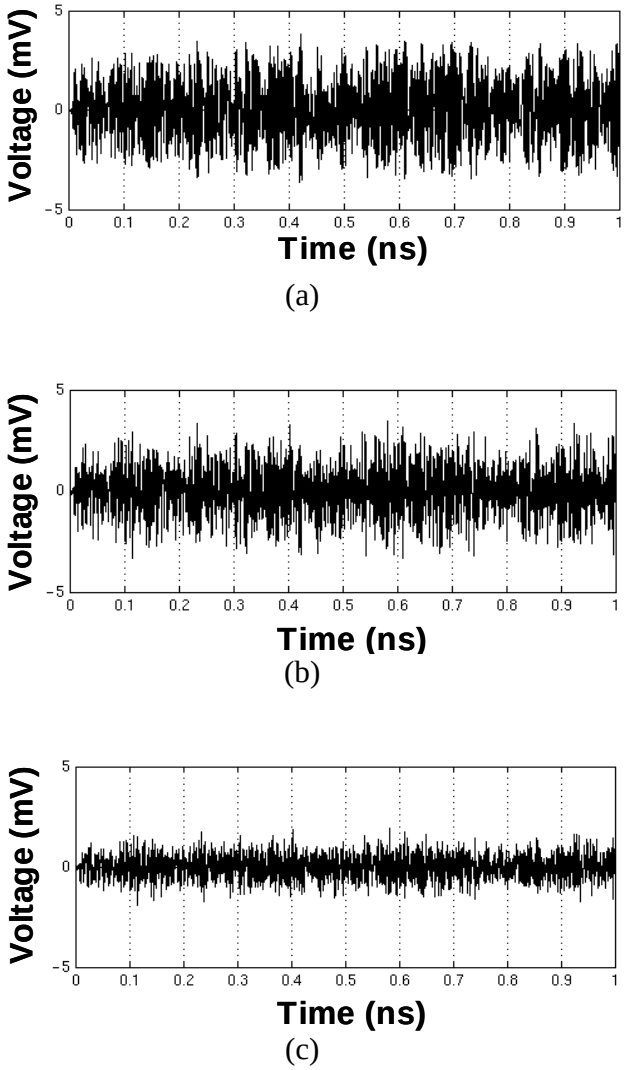


Figure 3.23. Waveforms of (a) the original NEXT noise, (b) the residual noise after coarse cancellation and (c) the residual noise after the fine cancellation.

Furthermore, Figure 3.23 shows the noise cancellation performance of the suggested NEXT noise cancellation technique. The power of the original NEXT noise shown in Figure 3.23(a), is halved after the coarse cancellation, as shown in Figure 3.23(b). This residual noise power is reduced with the fine cancellation and halved again as shown in Figure 3.22(c). As a result, the corresponding SNRs are improved by 3 dB for each cancellation procedure. In other words, the suggested NEXT noise cancellation technique provides the overall SNR improvement of 6 dB, as shown in Figure 3.23 (c).

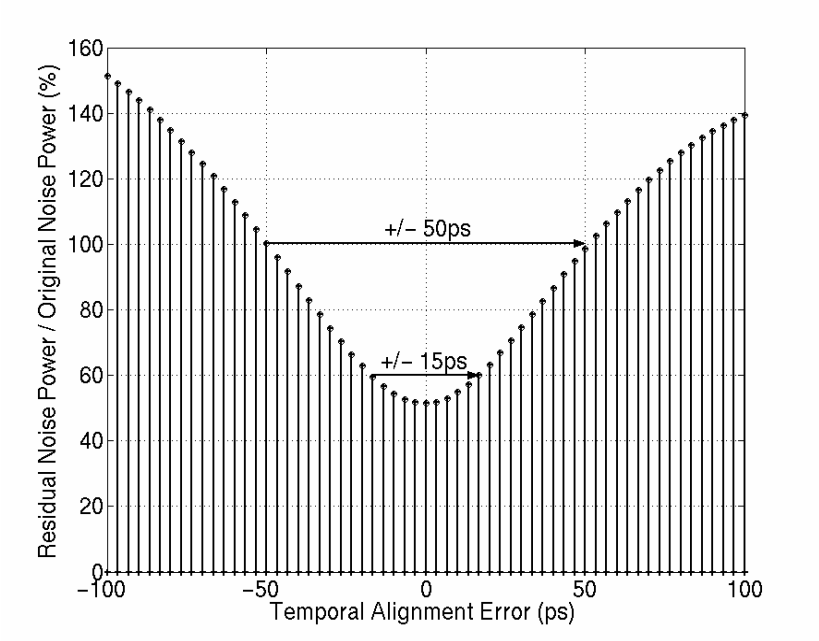


Figure 3.24. Ratio of residual NEXT noise power after a coarse cancellation to the original NEXT noise for different amount of temporal alignment error.

Another important function of the NEXT noise canceller is a temporal delay alignment, which compensates for the propagation delays induced through the daughter card trace and connectors. Figure 3.24 shows the ratio of residual NEXT noise power after the coarse cancellation to the original NEXT noise for different amount of temporal

alignment error. To investigate the optimum specifications of the temporal alignment delay line, this simulation assumes a perfectly matched coarse emulation filter. From the Figure 3.24, the proposed NEXT noise cancellation technique requires the temporal delay alignment error must be within 15 ps.

3.3. SYSTEM CONFIGURATION SUMMARY

In the previous sections, the system architectures of the suggested equalization and NEXT noise cancellation were provided, and the corresponding building blocks were simulated to investigate the corresponding optimum specifications. This section summarizes the whole system specifications of the combined solution of the suggested equalization and the NEXT noise cancellation technique. Moreover, the system architecture of this combined system solution is illustrated with the system model of the backplane channel configuration.

Table 3.1. The summary of the suggested system specification

Backplane Channel	Dielectric	FR-4
	Trace Length	20 in
	Connector	Type A, B, and C
Signaling	Data Throughput	20 Gbit/sec
	Modulation	4-PAM
	Bandwidth	10 GHz
Equalization	Type	RX-FFE (MMSE-LE)
	Structure	4-tap FIR (Tap-spacing : 33 ps)
NEXT Cancellation	Coarse channel filter	Tunable PZ filter
		Corner frequency : 2~5 GHz
	Fine channel filter	7-tap FIR (Tap-spacing : 33 ps)
	Temporal alignment delay line	15 ps/stage, 7 stages

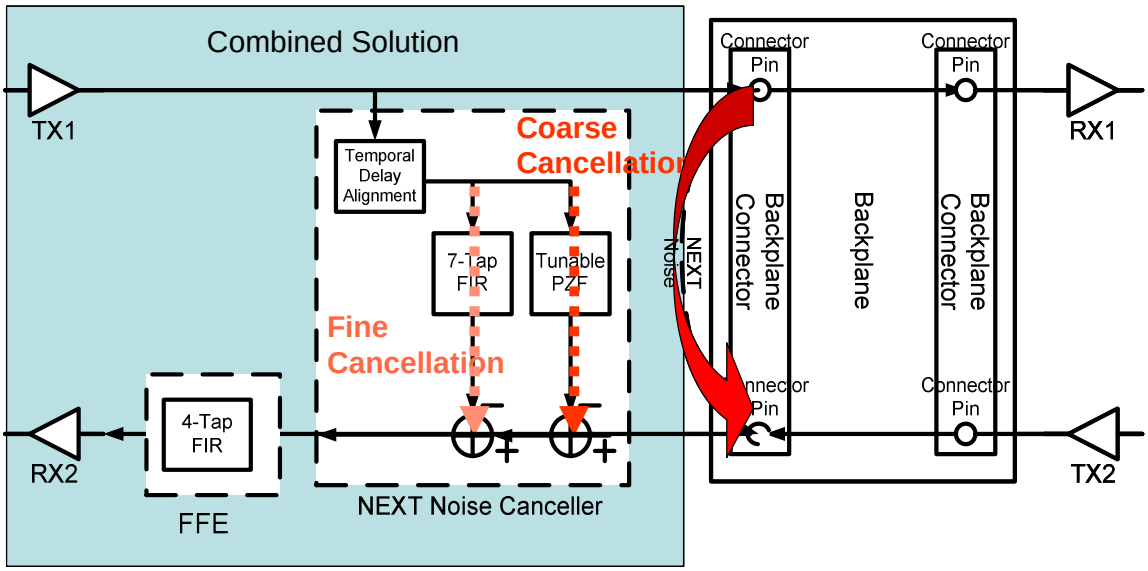


Figure 3.25. Functional block diagram of the proposed equalization and NEXT cancellation technique.

CHAPTER IV

CMOS IC IMPLEMENTATION

In this chapter, the IC implementation of the suggested FFE and NEXT noise cancellation technique will be discussed in detail. First of all, practical IC design issues such as bandwidth, voltage headroom, and the selection of fabrication process are discussed in section 4.1. As investigated from the previous chapter, the FFE is consisted of the building blocks such as the tap delay line and variable gain amplifiers. Section 4.2 provides the circuit topologies and simulation results for these building blocks of the FFE. Additionally, several design skills to address the implementation challenges for the FFE will be described. In section 4.3, the details of the IC design of the NEXT noise cancellation IC are offered. The circuit topologies of each building block, i.e. the tunable PZ filter and the 7-tap FIR filter, the temporal alignment delay line are discussed. Moreover, their performances are simulated and the corresponding results will be verified with the measurement results in section 4.4. The section 4.4 introduces the experiment setups for the measurement of the fabricated ICs as well as the measurement procedures in detail. The building blocks of the FFE and the NEXT noise cancellation IC are characterized to verify if these fabricated ICs meet the requirements investigated in the system simulation as well as the circuit simulation. Then, the measured system performances of equalization and NEXT noise cancellation of the implemented ICs are presented.

4.1. CIRCUIT DESIGN CONSIDERATION

Before discussing the details of the IC designs, it is very important to consider practical issues expected in the IC implementation. Selecting the adequate fabrication process technology and the signaling scheme may establish the intrinsic technical limitations in the IC implementation. Thus, practical IC design issues such as bandwidth, linearity, voltage headroom, and noise immunity are reflected to come up with the corresponding optimum circuit topologies for the technical challenges. This section discusses the practical circuit design issues considered to realize the suggested FFE and the NEXT noise cancellation Technique.

Differential signaling and differential-ended circuit topologies exploit their intrinsic immunity to external interference as well as to their lower voltage swing resulting in lower power consumption. These beneficial features are major reasons that the differential-ended topology was adopted in the IC implementation for this work. Meanwhile, multi-level signal scheme such as 4-PAM signaling must be amplified with quite linear gains to avoid clipping phenomena due to nonlinear gain characteristics of amplifiers. Thus, linearity requirement is more strictly applied to the IC design in this work. Moreover, broadband circuit topologies are needed to handle the 10-GHz bandwidth signal with little transient response impairment. The bandwidth-enhanced circuit topologies are investigated and adopted in this work.

For signal integration with digital circuitry, CMOS process technology is adopted for IC implementation. Especially, all the building blocks are implemented using a 0.18-um CMOS process with operating power supply voltage 1.8 V. Therefore, a voltage-

headroom is one of the critical design issues to guarantee high speed signal processing with linear circuit operations.

The proposed FFE and NEXT noise canceller adopt the FIR filters with four and seven taps separated by $T_S/3$ (i.e. 33 ps), respectively. In order to implement the FIR filter structure, a tap delay line using passive LC artificial transmission line can be adopted to deliver broadband signal due to the peaking feature of inductors. However, the series resistance of the passive inductor inevitably induces DC voltage drops and signal power loss across each stage. This feature can be the main problem to implement the analog FIR filter with large number of taps. In this work, an active delay line is employed to overcome the problems of this passive delay line approach. The penalty over passive delay lines, however, is bandwidth impairment issue. Therefore, the bandwidth-enhancement circuit topology is suggested and applied in this work. Linear amplification of tap gain amplifier is another critical requirement. Linear gain control topology is investigated and its performance is tested in this work. Moreover, the PZ filter for the NEXT noise cancellation should be adjusted to the different connectors' channel responses. Thus, tuning feature is adopted and examined to adjust the corner frequency of the PZ filter response.

In the following section 4.2 and section 4.3, the FFE IC and the NEXT noise canceller building block ICs implemented in a standard 0.18-um CMOS process will be discussed in detail.

4.2. CMOS FEED-FORWARD EQUALIZER (FFE)

The suggested FFE is the FIR filter with four tap coefficients and $T_s/3$-tap spacing. All four tap-coefficients are derived with the MMSE algorithm, and 33-ps of delay per stage is adopted for the fractional-spaced equalization as mentioned previously. The active delay line is composed of four unit delay cell. Each unit delay cell is consisted of three stages of cascaded differential pair amplifiers.

Figure 4.1 shows the block diagram of the fully integrated FFE IC. All the building blocks are integrated with a 0.18-μm standard CMOS process.

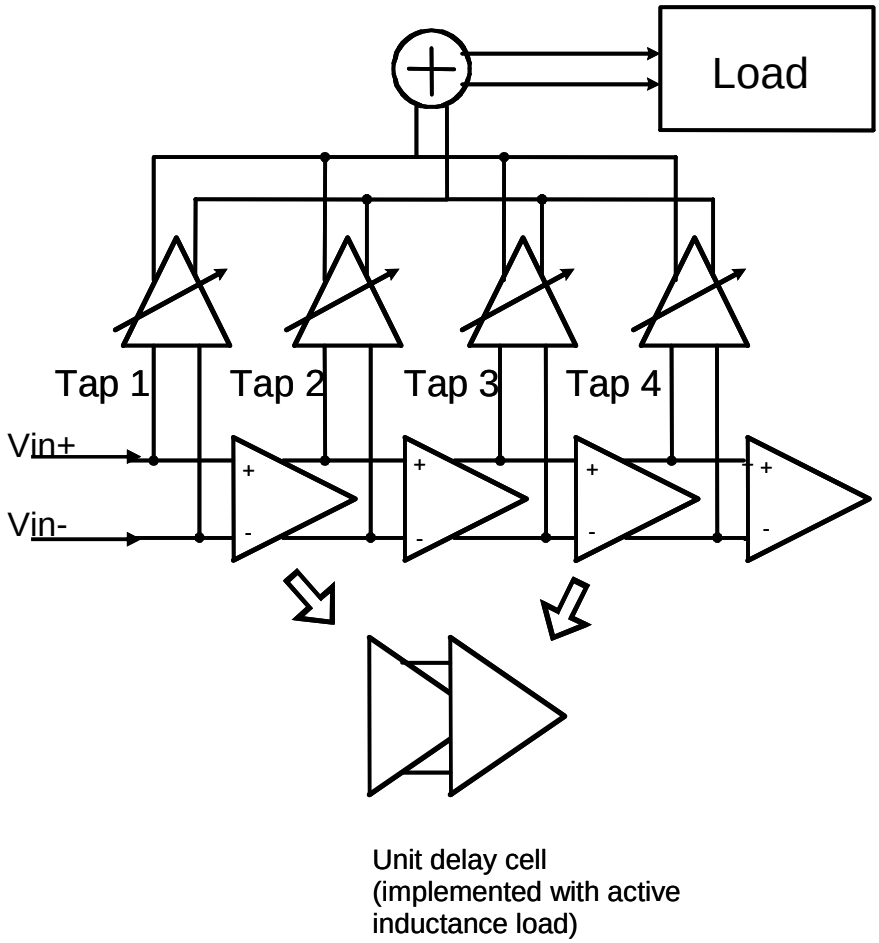


Figure 4.1. Block diagram of the fully integrated FFE IC.

In the following sections, each circuit building block of the FFE will be described in detail. In the section 4.2.1, the multiplier cell will be covered for the tap gain amplifier. The section 4.2.2 describes the active delay line circuit design including various bandwidth-enhancement skills. Moreover, a bias method immune to power supply noise will be discussed.

4.2.1. MULTIPLIER CELL

In order to realize bi-polar linear gain features, the Gilbert cell is used as a multiplier cell for the equalizer. The major function for the multiplier cell is to adjust the amplitude of the signal coming from each delay cell output. The simplest way for the gain variation is to control the bias current in a simple differential pair as shown in Figure 4.2 (a). The gain is proportional to the square-root of a bias current. This current sink control method is simple to implement. However, it still has undesirable characteristics such as the output common mode voltage variation depending on the gain variation. The other gain control technique is to vary the degeneration resistance as shown in Figure 4.2 (b). The voltage gain for the source-degenerated differential pair is calculated as in eq. (4.1).

$$\frac{g_m}{1+g_m R_s} R_d \qquad \text{eq. (4.1)}$$

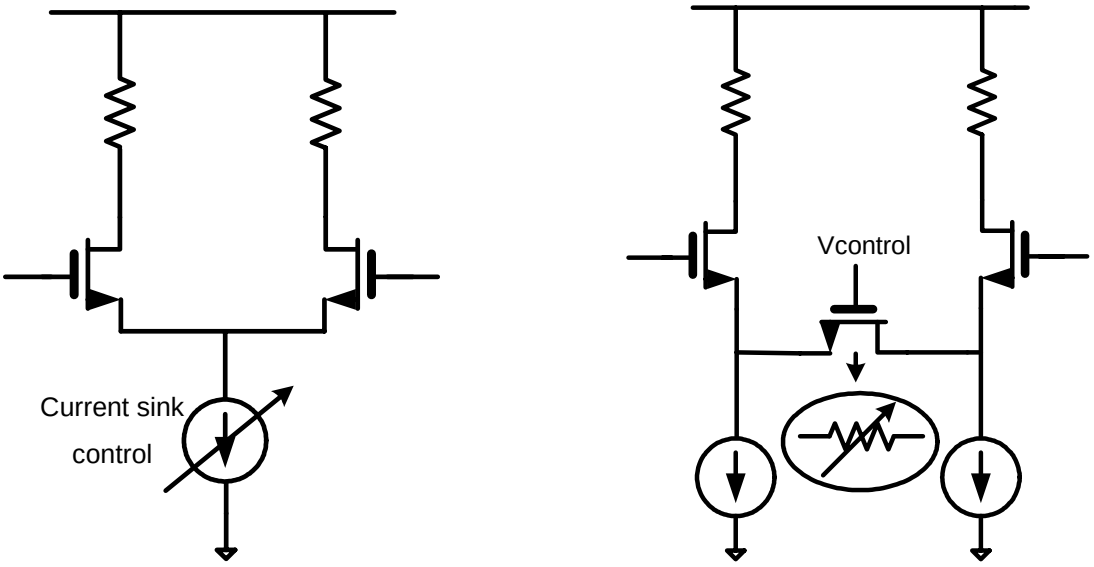
,where g_m, R_s and R_d are the trans-conductance of the NMOS, the degeneration resistance and the load resistance, respectively. By changing the R_s, the overall voltage gain can be varied without changing the common mode output voltage. The variable resistor can be implemented by using on-resistance of the MOS. The bias condition for this on-resistance of the MOS is that the MOS operates in triode region (i.e. $V_{ds} > V_{gs} - V_t$, where V_{ds} is the

drain-source voltage and V_t is the threshold voltage for the MOS). The on-resistance of the MOS is shown in eq. (4.2).

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)} \qquad \text{eq. (4.2)}$$

,where μ_n, C_{ox}, W are the mobility of the electrons, the gate oxide capacitance per unit area, and the MOS width and L is the MOS channel length, respectively.

By summary, the gain control can be implemented by ways of changing the bias current, degeneration resistance. However, single differential pair amplifier employing these methods can not offer the bi-polar gain feature required for the suggested FFE.



(a) (b)

Figure 4.2. Gain control methods for differential pair amplifier using (a) the current sink variation and (b) the source degeneration variation.

Due to the benefit of differential signaling, the bi-polar gain is achievable by swapping the connection of differential pair as shown in Figure 4.3. The two differential pair

amplifiers are tied together at their drain nodes with opposite signal polarity. This is the conventional Gilbert cell structure. Because of this bi-polar gain control feature, the Gilbert cell structure was adopted as the tap gain amplifier for the suggested FFE.

For high-speed circuit operation, passive loads are chosen instead of active loads as current summation node. However, despite the bandwidth advantage of the passive resistance loads, the open drain connection of the conventional Gilbert cells to the resistive load induces the voltage headroom issue, i.e. the voltage drop across the passive load increases linearly as the number of tap increases. This voltage drop forces the transistors M1, M2, M3 and M4 to operate in the triode region.

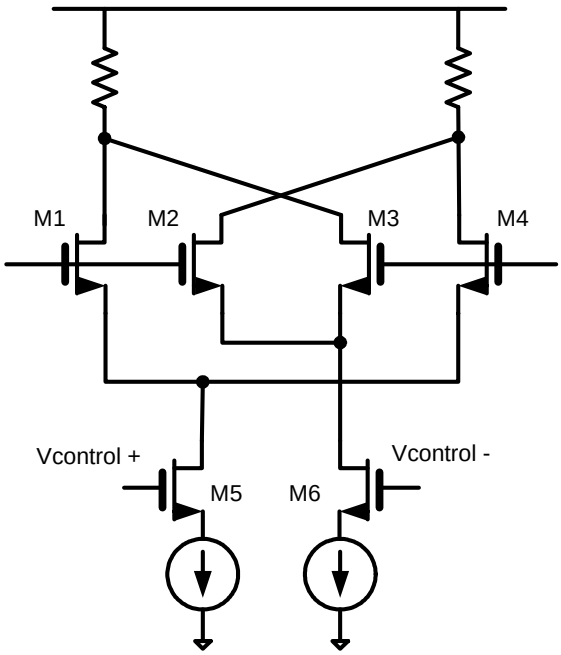


Figure 4.3. Conventional Gilbert cell topology.

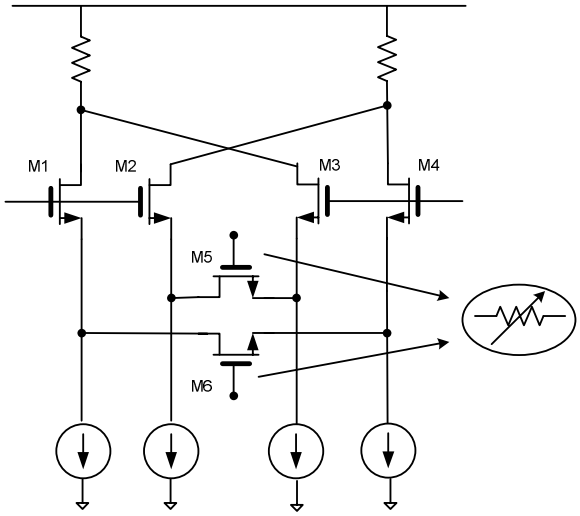


Figure 4.4. Gilbert cell with variable source degeneration.

Besides on this current steering technique, another way of implementing low voltage Gilbert cell operation is reported [32], as shown in Figure 4.4. The gain variation by varying the degeneration resistance enables to remove the differential pair (M5, M6) in Figure 4.3. Replacing the three stacks of transistor to two transistors via source degeneration results in reduced voltage headroom consumption as well. The source degeneration variable resistance method has comparable voltage headroom consumption with the modified Gilbert cell structure because of identical number of transistor stacks. However, the method shown in Figure 4.4 has some potential gain symmetry problems. M5 and M6 have to have odd-symmetrical turn-on resistance relation, however the on-resistance has reciprocal relation to the gate voltage making it difficult to maintain odd-symmetry relation. In order to compensate the non-linear resistance, the gates of M5 and M6 are connected to the gates of M1 and M3, respectively. As gate voltage of M1 becomes more positive than the gate voltage of M3, transistor M3 stays in the triod region because VD3 = VG3-VGS1 whereas M4 eventually enters the saturation region

because its drain voltage rises and its gate and source voltages fall. Thus, circuit remains relatively linear even if one degeneration device goes into saturation. Instead of using the upper four transistors (i.e. the M1, M2, M3, and M4 in Figure 4.4) as the signal input, *Wu et al.* [18] introduced the way using upper four transistors as switch to set the gain polarity and the current sink for gain variation as shown in Figure 4.5. This method has advantage that the output loading effect is minimized, because two of upper four transistors are always on and the others are always off, which is independent of the gain value. However, as mentioned earlier, current sink control method has potential undesirable effect that the output common mode voltage can be changed as the gain changes.

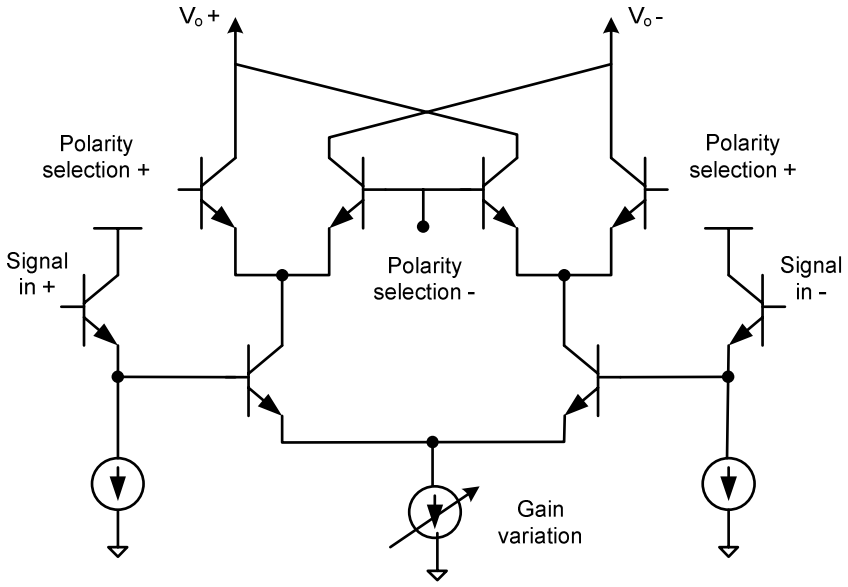


Figure 4.5. Gilbert cell using the upper transistor as switches.

To address the voltage headroom issue of the conventional Gilbert cell, a modified Gilbert cell is newly proposed as shown in Figure 4.6. This multiplier cell uses a folded

gain control circuit with the bias current block folded as well. The mirror pole capacitance at the AC ground node in the proposed multiplier cell has negligible effect on the overall bandwidth performance since the gain control signal path does not require high speed performance. Transistor M5, M6, M7 and M8 are used for active degeneration in order to achieve linear gain performance [33]. Moreover, the gain control block adopted a degeneration scheme, M11 and M12, for linear gain.

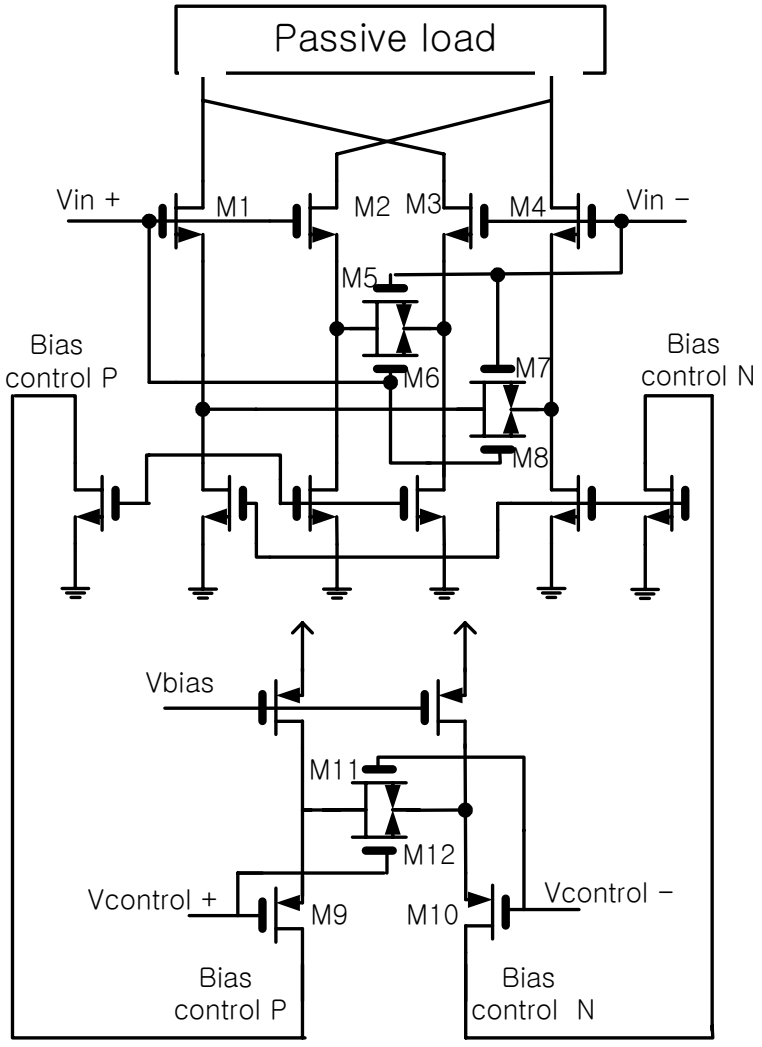
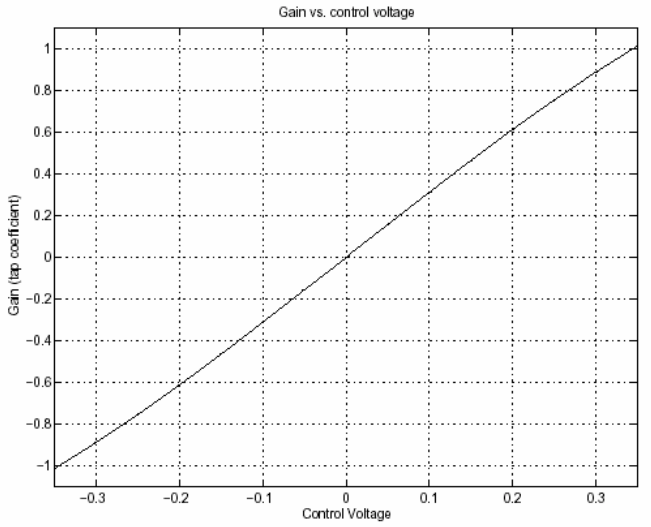
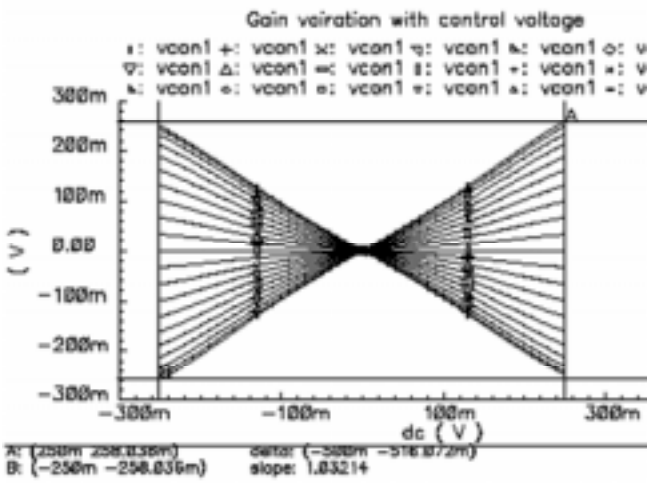


Figure 4.6. Modified Gilbert cell with folded gain control block.



(a)



(b)

Figure 4.7. DC gain characteristic of the modified Gilbert cell. (a) DC gain variation vs. control voltage of the multiplier cell. (b) DC gain curve of the modified Gilbert cell showing input dynamic range with linearity across control voltage.

The gain characteristic is simulated for the modified Gilbert cell as shown in Figure 4.7(a). This simulation result shows the linear gain performance for the gain control voltage of -300 mV ~ 300 mV. Figure 4.7(b) shows the DC gain curve of the multiplier cell structure demonstrating the maximum peak-to-peak input signal voltage level for its

linear operation. The input dynamic range is increased by use of the active source degeneration circuit M5, M6, M7, and M8 in Figure 4.6.

4.2.2. ACTIVE INDUCTANCE PEAKING DELAY LINE

The suggested active delay line is implemented with several cascaded stages of differential amplifier cells. The propagation delay is generated by the RC transient characteristic, i.e., the load resistances and gate capacitances of the differential amplifier cells. These differential amplifier cells are designed to have unity gain and constant common DC voltage through each stage. Moreover, its delay values can be changed by controlling the bias voltage of the active load transistor. The penalty over passive delay lines, however, is increased power consumption. Futhermore, it is more challenging to satisfy the bandwidth requirements for 10-Gbit/sec signal handling over the passive delay line counter part. In this section, various bandwidth enhancement methods will be covered briefly. Specifically, active inductance approach will be presented in detail.

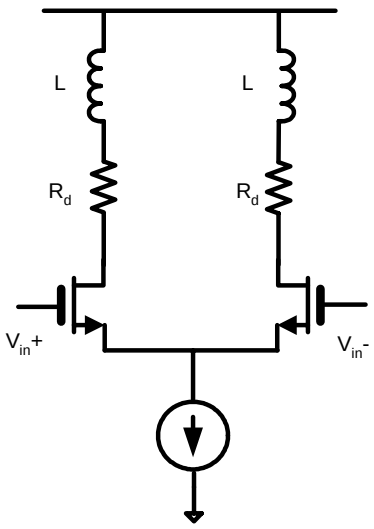


Figure 4.8. Peaking inductance to enhance the bandwidth.

The most well-known bandwidth enhancement technique is to use shunt peaking inductor at the signal path. Figure 4.8 shows the example of the inductive peaking technique. Series connection with a resistor R_d generates zero at R_d/L in frequency domain. By controlling the inductance value, the frequency peaking range can be determined.

Another bandwidth enhancement technique is to add the capacitance in series with the input gate-source capacitance. Therefore, the input capacitance of the given stage can be reduced by half. As shown in Figure 4.9, two differential pairs are connected in series at the input and in parallel at the output port. The overall voltage gain is same as the one of single differential pair. However, the input capacitance is reduced by half (C_{gs} /2, where C_{gs} is the gate-source capacitance of four NMOS in two differential pairs). Because the circuit structure has the half input capacitance, it is called F_t doubler [34]. In spite of the benefit of the reduced input capacitance, this structure has several drawbacks compared to the simple differential pair. The total power consumption is doubled due to the additional current sink. The current flow at the resistive load is increased by twice, increasing the voltage drop, which tends to force the four NMOSs in two differential pair working in the triode region. Therefore, this structure reduces the output voltage swing as well as the input dynamic range. Finally, the C_{ds}, and C_{gd} of the current sink transistor increase the input capacitance from the ideal value of C_{gs} /2.

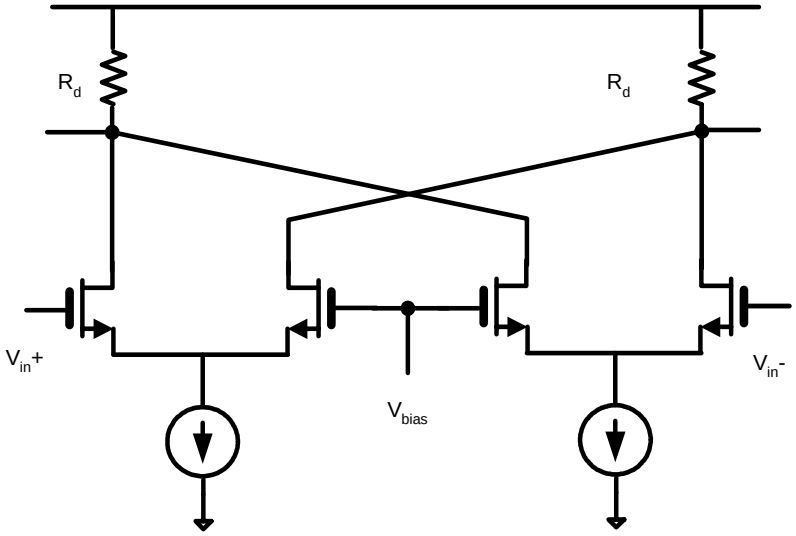


Figure 4.9. F_t doubler.

In order to create broadband characteristic, it is possible to degenerate the transistor in a way to increase their trans-conductance as the operation frequency is increased. Therefore, it compensates the high-frequency roll-over resulting in bandwidth enhancement. Figure 4.10 shows the one example of capacitive degeneration in differential pair. Using the half circuit of the Figure 4.10, the voltage gain can be expressed as in eq. (4.3).

$$A_v = \frac{R_d \| \frac{1}{sC_L}}{\frac{R_s}{2} \left\| \frac{1}{2C_s s} + \frac{1}{g_m} \right.} \qquad \text{eq. (4.3-a)}$$

$$= \frac{g_m R_d (sC_s R_s + 1)}{(1 + sR_d C_L)(g_m R_s / 2 + 1 + sC_s R_s)} \qquad \text{eq. (4.3-b)}$$

The voltage gain has zero at the $1/C_sR_s$ and two poles at $1/R_dC_L$ and $[g_m R_s/2+1]/C_sR_s$. By controlling the degeneration capacitance C_s, the peaking can be located at the desired frequency or cancel the dominant pole resulting in increased bandwidth.

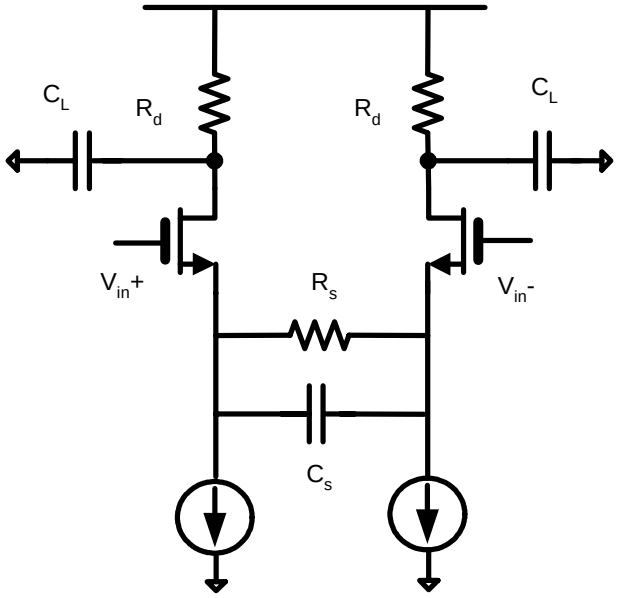


Figure 4.10. Capacitive degeneration.

Additionally, the Cherry-Hooper amplifier is introduced as a bandwidth-enhancement circuit topology [35]. Figure 4.11 shows the example of the Cherry-Hooper amplifier topology with ideal current source as the load. From the simple calculation, the voltage gain for the Cherry-Hooper amplifier topology is shown in eq. (4.4).

$$g_{m1}(R_d - \frac{1}{g_{m3}}) \qquad \text{eq. (4.4)}$$

As far as $R_d >> 1/g_{m3}$, the overall voltage gain is same as the one of a simple differential pair. Meanwhile, the output impedance of the Cherry-Hopper amplifier is approximately $1/g_{m3}$, which is usually smaller than MOS drain resistance r_d resulting in output pole location much far from the origin compared to the simple differential pair. The broadband characteristic of the Cherry-Hopper amplifier, more current consumption compared to the simple differential pair is the drawback of the Cherry-Hooper amplifier.

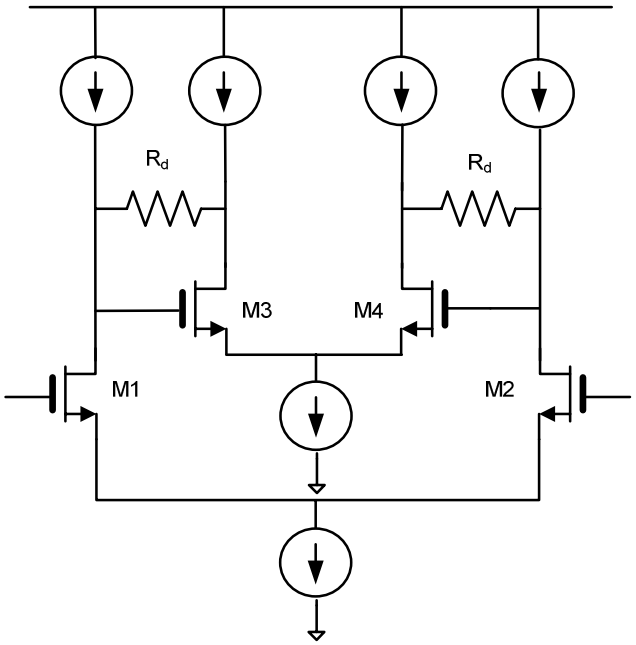


Figure 4.11. Cherry-Hopper amplifier topology.

Among the bandwidth enhancement topologies introduced in this section, shunt inductance peaking topology consumes relatively low power. Thus, this topology was applied to the active delay line cell. However, as mentioned earlier, the on-chip passive inductor is still requiring large CMOS chip space. In order to reduce the die area and to realize the adjustable delay feature, the source follower was chosen as a load replacing the series combination of on-chip inductor and resistor.

Figure 4.12 shows the fully integrated FFE IC architecture with the proposed active delay line structure. The overall voltage gain for differential pair in unit delay cell is expressed in eq. (4.5).

$$A_v = g_{m3} \cdot (Z_{in} // C_L) \qquad \text{eq. (4.5-a)}$$

$$= \frac{sC_{gs2}R_s g_{m3} + g_{m3}}{C_{gs2}C_L R_s s^2 + (C_{gs2} + C_L)s + g_{m2}} \qquad \text{eq. (4.5-b)}$$

,where $C_L = C_{gd3}(1+A_v) + C_{db3}$, and $Z_{in} = \dfrac{sC_{gs2} \cdot R_s + 1}{sC_{gs2} + g_{m2}}$ eq. (4.6)

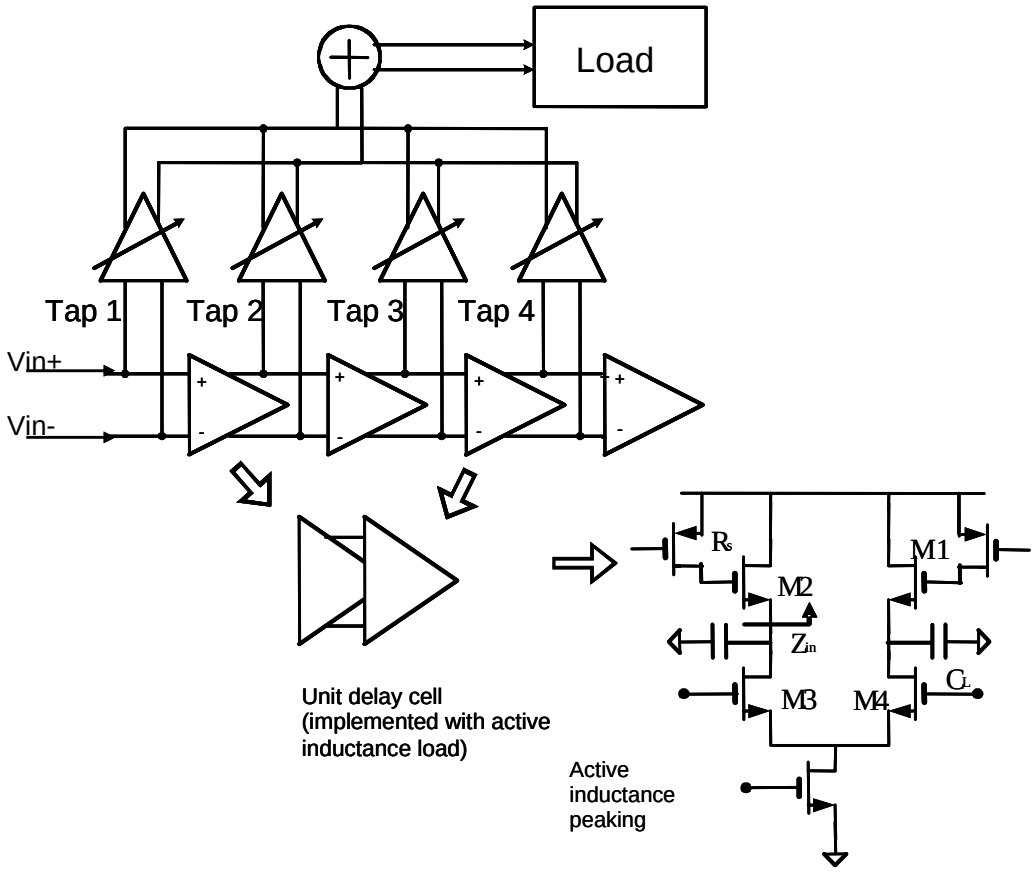
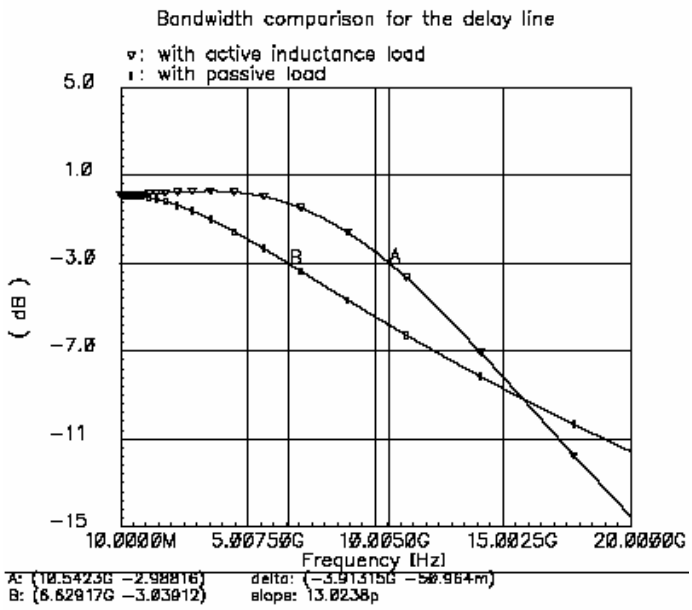


Figure 4.12. Fully integrated FFE IC architecture with proposed active delay line structure.

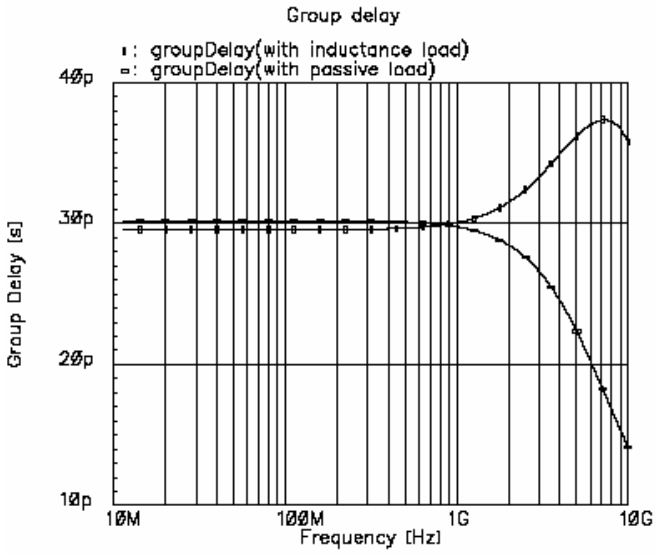
The two poles are located at $-\frac{1}{2}(\frac{C_{gs2}+C_L}{C_{gs2}C_L R_s}) \pm \frac{1}{2}\sqrt{(\frac{1}{C_L R_s}+\frac{1}{C_{gs2}R_s})^2 - \frac{4g_{m2}}{C_{gs2}C_L R_s}}$ and the zero is placed at $\frac{1}{R_s C_{gs2}}$. By varying the R_s, (R_s is turn-on resistance of M1 in Figure 4.12.) the zero location can be controlled. To reduce the external voltage source for the equalizer, turn-on resistance is replaced by passive resistance in this design. Figure 4.13

shows the simulated bandwidth characteristics of the active delay lines with passive resistor load and with active inductance load. The active inductance load enhances the 3-dB bandwidth of the delay line by approximately 3.9 GHz compared to passive resistor load. For the fair comparison, the group delay for the passive resistor load and the active inductance load are set to the same amount. Also the gain for the delay line is set to unity for both the cases. The simulation includes all the parasitic capacitances from the multiplier cell and the adjacent delay cell.

For the active delay line implementation, two cascaded NMOS differential pairs are used generating 33-ps delay per unit delay cell. The effective inductance value, which is proportional to $R_s/(1/g_{m2})$, is optimized for 10 Gbit/sec NRZ signal transmission. In Figure 4.14, the transient simulation result for the designed FFE IC shows 4-GHz bandwidth improvement with the active inductive load. The relative delay between the adjacent taps is optimized to be 33 ps.



(a)



(b)

Figure 4.13. Bandwidth comparison between the passive load and active inductance load. (a) The 3-dB bandwidth comparison between passive load and active inductance load. (b) Group delay for the passive load and active inductance load.

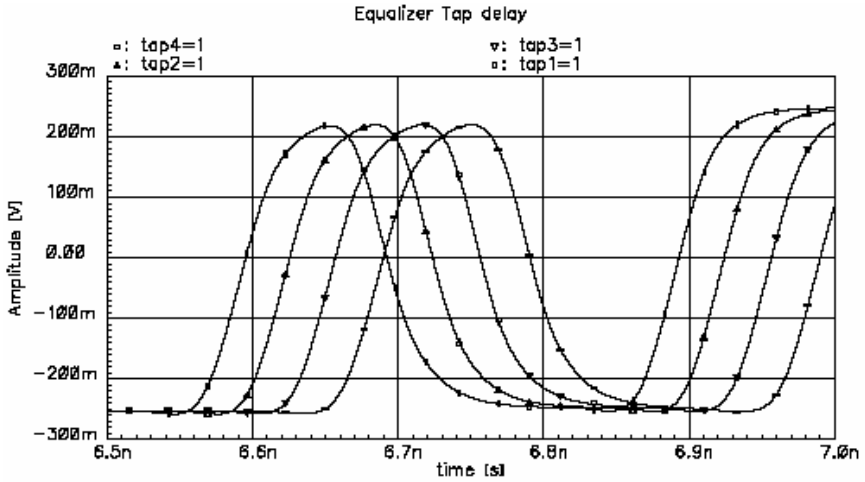


Figure 4.14. Delay line performance with 33-ps continuous-time tap delay.

4.2.3. POWER SUPPLY NOISE IMMUNE BIAS SCHEME

The reference current source is generated using the supply noise rejection bias scheme as shown in Figure 4.15 [36]. For given power supply voltage variation ΔV_{dd}, the corresponding reference voltage variation ΔV_{ref} is calculated as in eq. (4.7).

$$\Delta V_{ref} = (\Delta V_{dd} - \Delta V_{pmos}) \frac{Z_2}{Z_1 + Z_2} \qquad \text{eq. (4.7)}$$

The resulting sensitivity of the V_{ref} to V_{dd} is reduced by a factor of ΔV_{dd}-ΔV_{pmos}. Consequently, the reference current I_{ref} is V_{ref}/R, where R is the resistance connected to the source of the NMOS. As a result, the reference current sensitivity to V_{dd} is also reduced with a same scaling factor as the ratio of V_{ref} to V_{dd}. This noise immunity improved reference current is used for the FFE building blocks, i.e. the unit delay line cell and multiplier cell. The reciprocal relation between the reference current and the

resistance reduces any undesirable resistance variation effects on a differential pair. Moreover, the current sink is mirrored with reference current and passive resistance is used as a load. The improved noise rejection from the power supply (V_{dd}) reduces the tail current noise in the delay line cell as well. As the time delay is proportional to 1/gm of a NMOS load in unit delay line cell, it alleviates any jitter coming from the power supply noise in the delay line cell.

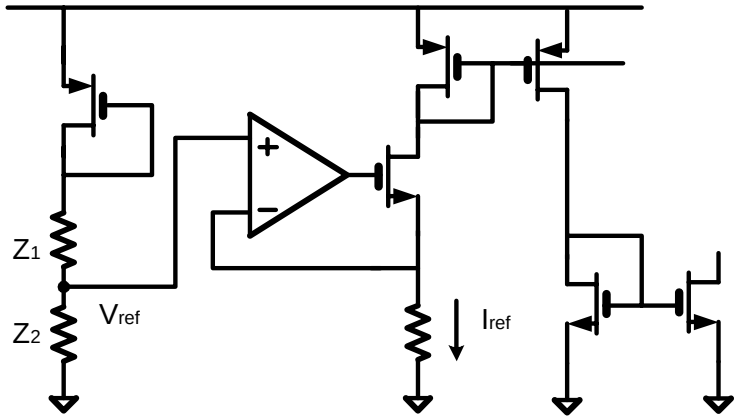
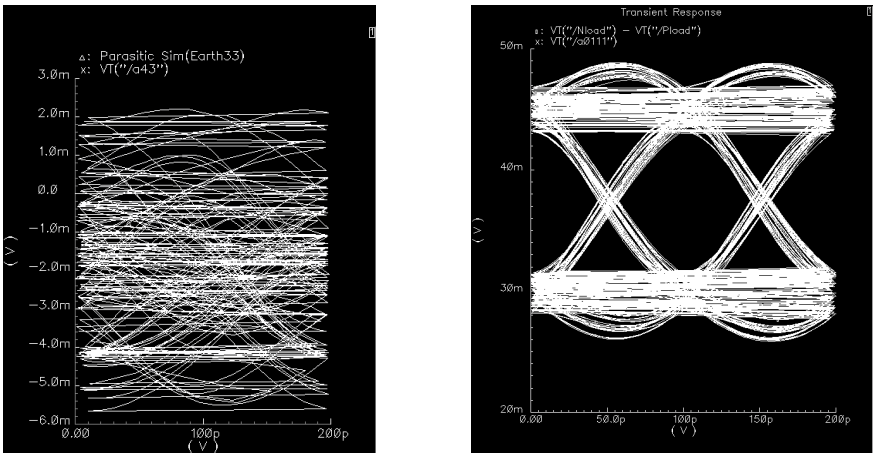


Figure 4.15. Noise rejection enhanced bias scheme.

4.2.4. FFE IC PERFORMANCE SIMULATION

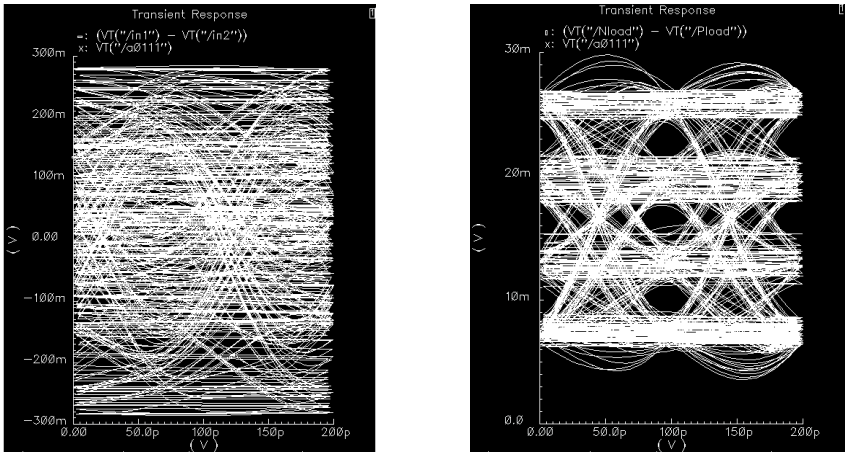
In the previous sections, tap delay and gain characteristics of the 4-tap FIR filter were simulated to verify its basic functions required from the system simulation. In this section, the circuit simulation is performed to verify the equalization performance for the 10-Gbit/sec NRZ and 20-Gbit/sec 4-PAM transmission over 20-in FR-4 backplane channel. The tap gain values from the system simulation for this channel are applied to

compensate the channel loss effect. The channel output signals are emulated with the measured channel characteristics and applied to the designed FFE IC as input signals. The channel output signal is delayed through the designed tap-delay line and amplified with the pre-determined tap gain values by the multiplier cells. Figure 4.16 (a) shows the eye diagram of the 10-Gbit/sec NRZ output signal from 20-in FR-4 backplane channel. Figure 4.16 (b) shows that the designed FFE IC compensates the channel loss and achieves the wide eye-opening. This eye-opening size is a metric of error performance in data transmission. Thus, this wide eye-opening guarantees the error-free data transfer through the backplane channel. Figure 4.17 shows the equalization performance for 20-Gbit/sec 4-PAM signal transmission through the 20-in FR-4 legacy backplane channel. From Figure 4.17 (b), the designed FFE IC is verified to be able to compensate the channel loss effect successfully for 20-Gbit/sec 4-PAM transmission.



(a) (b)

Figure 4.16. Simulated eye diagrams of 10-Gbit/sec NRZ signal (a) before and (b) after equalization by the designed FFE IC for 20-in FR-4 legacy backplane channel.



(a) (b)

Figure 4.17. Simulated eye diagrams of 20-Gbit/sec 4-PAM signal (a) before and (b) after equalization by the designed FFE IC for 20-in FR-4 legacy backplane channel.

4.3. CMOS NEXT NOISE CANCELLER

As mentioned in the section 4.1, the NEXT noise cancellation IC should be able to provide the tunable feature for the channel emulation for the different connector types. Therefore, the NEXT channel emulation filters, i.e. PZ filter and 7-tap FIR filter, are designed to be adjustable by the control values. Moreover, the 7-tap FIR filter and the temporal alignment delay line have severe loading effects due to the large number of taps connected directly to each other. In order to overcome this bandwidth challenge, various technical efforts are introduced in the design of those two building blocks. The following sections present the details of circuit design and the topologies of each building block and the corresponding simulation results are presented.

4.3.1. TUNABLE POLE-ZERO (PZ) FILTER

A tunable active PZ filter circuit handles the coarse cancellation. Gain and corner frequency are adjustable to match the low frequency response of the NEXT channel. PZ filter circuit schematic is shown in Figure 4.18. Transistor M1 is connected in a common drain configuration with no AC ground between the drain and the current sink. Lacking viable varactor structures in the CMOS process, the corner frequency is determined by the resistance of the active load. The load consists of a differential active load [37] to maintain constant DC levels at the output for different loads. Transistor M4 and M5 set the DC and common voltage. The static resistors and transistor M3 determine the differential load that appears at the output. Varying the bias at the gate of M3 adjusts this differential load.

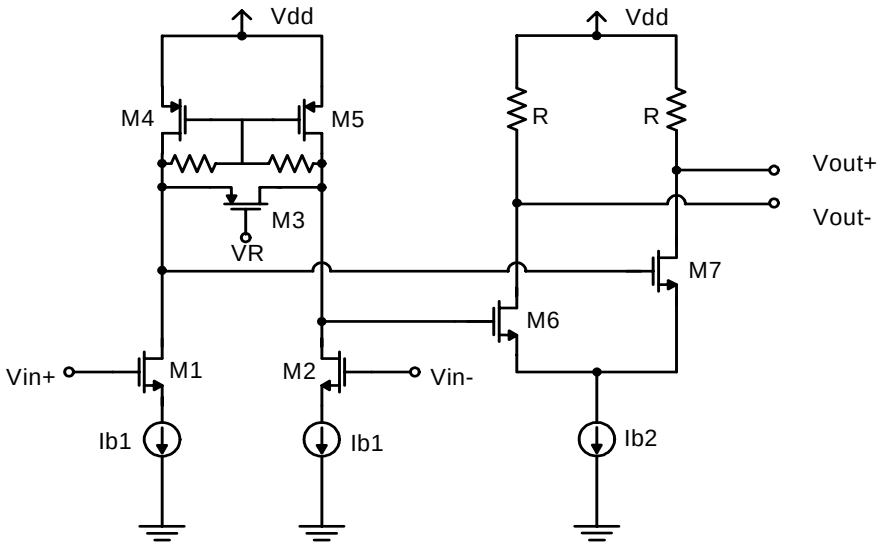


Figure 4.18. Schematic of the proposed tunable active PZ filter.

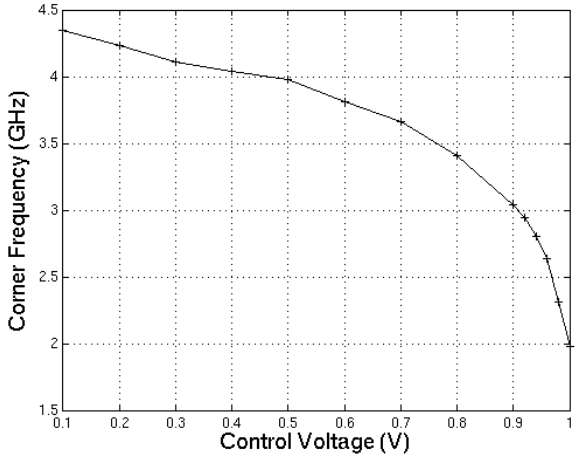


Figure 4.19. Corner frequency of the tunable active PZ filter

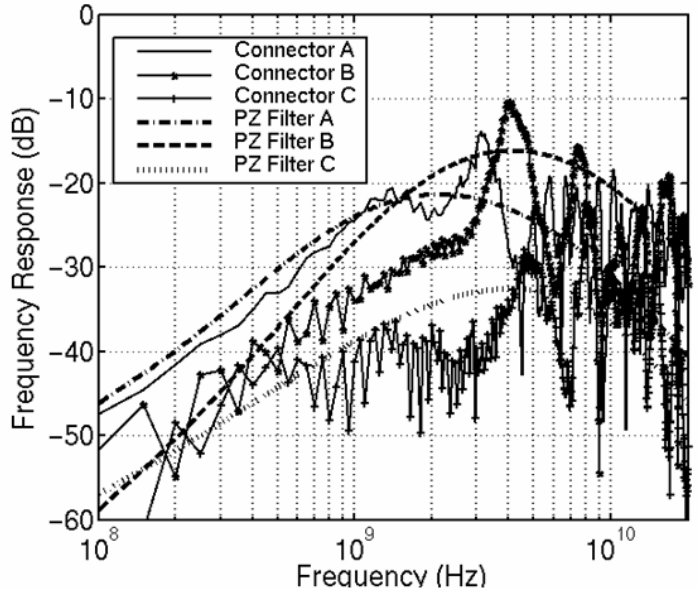


Figure 4.20. Frequency responses of the PZ filter tuned to match the characteristics of three different channels shown in Figure 2.9

Figure 4.19 illustrates the tuning range of the proposed active tunable PZ filter. Over a 1-V control voltage range, the corner frequency can be adjusted from 2 GHz to 4.4 GHz. Additionally, Figure 4.20 demonstrates the tunable response of the PZ filter and how it can be adjusted to match the characteristics of three different channels shown in Figure 2.9.

4.3.2. 7-TAP FIR FILTER

From system simulations in the section 3.2.3, the optimum architecture of the analog FIR filter for the fine channel emulation filter is determined to have 7 taps with 33ps tap spacing, and its block diagram is shown in Figure 4.21.

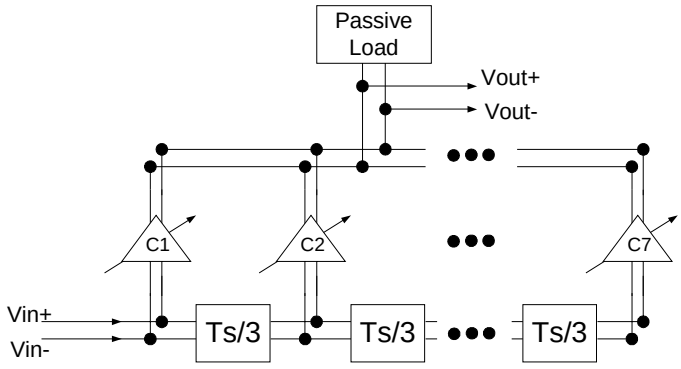


Figure 4.21. Functional block diagram of the 7-tap FIR filter.

The building blocks are a seven-stage tap delay line and seven multipliers for each tap. These building blocks have the same structures as the ones used in the 4-tap FIR FFE. However, the number of taps is increased from four to seven. The resulting output signals from these seven taps are connected to the output load directly. The corresponding

loading effect is increasing and results in bandwidth impairment. Thus, the layout of 7-tap FIR filter was carefully performed to reduce the undesired parasitic effects as shown in Figure 4.22.

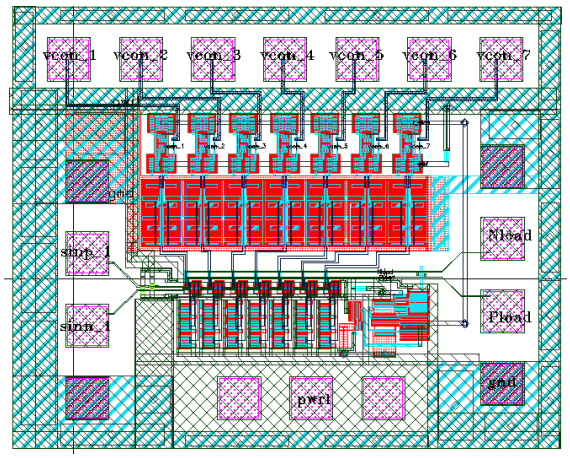
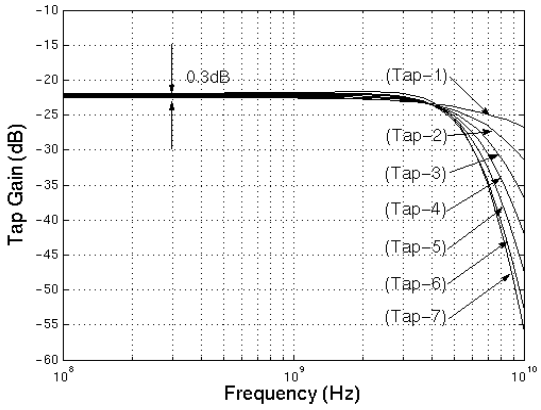
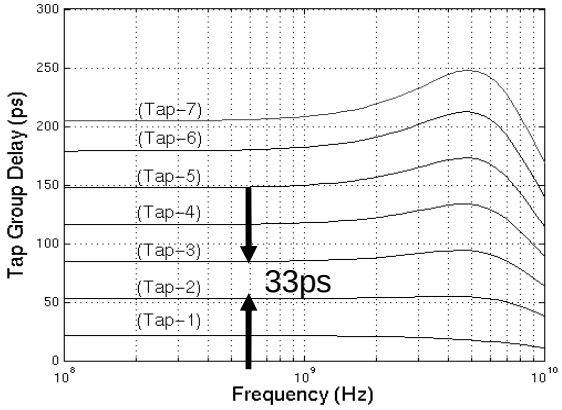


Figure 4.22. Layout of the 7-tap FIR filter circuit.

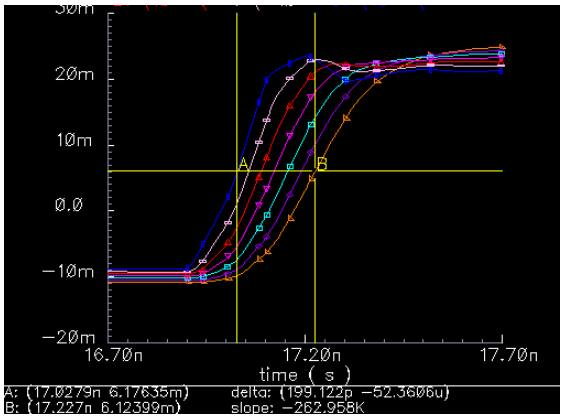
As the number of taps increases, the parasitic capacitance and resistance affect the circuit simulation results more severely. In order to improve the accuracy of the ideal circuit simulation without any parasitic effects from the actual layout, these parasitic values are extracted from the layout and reflected to the circuit simulation. Figure 4.23 shows the parasitic extracted simulation results of the designed 7-tap FIR filter. The tap gain characteristic, shown in Figure 4.23 (a), has a gain difference of 0.3-dB between the first and the seventh taps. Moreover, the 7-tap FIR filter provides a 3-dB bandwidth above 5.7 GHz for the worst case, i.e. the seventh tap. The group delay characteristics, shown in Figure 4.23 (b), have 33-ps delay between the adjacent taps, and its variation is smaller than 40-ps for the worst case. Figure 4.23 (c) shows the corresponding transient simulation result for the tap delay. The total delay value of 200 ps is achieved from the simulation of the designed 7-tap FIR filter IC.



(a)



(b)



(c)

Figure 4.23. Simulation results of (a) gain characteristics, (b) group delay characteristics and (c) tap delay of the designed 7-tap FIR filter circuit.

4.3.3. TEMPORAL ALIGNMENT DELAY LINE

A temporal alignment delay line is implemented with unit delay cells (DU), shown in Figure 4.12, and current mode logic switch circuitries, as shown in Figure 4.24. Seven blocks of the DU are cascaded to produce the required time delay of a symbol-duration (i.e. 100 ps). Each DU can be pulled out and connected to the next block. To control the amount of the delay value, differential pairs are used as the switch with the control at the current source. Figure 4.25 shows the corresponding simulation result of the designed temporal alignment delay line circuit. The result shows that the temporal alignment delay line can achieve tap delay values from 15 ps up to 100 ps with 15-ps resolution.

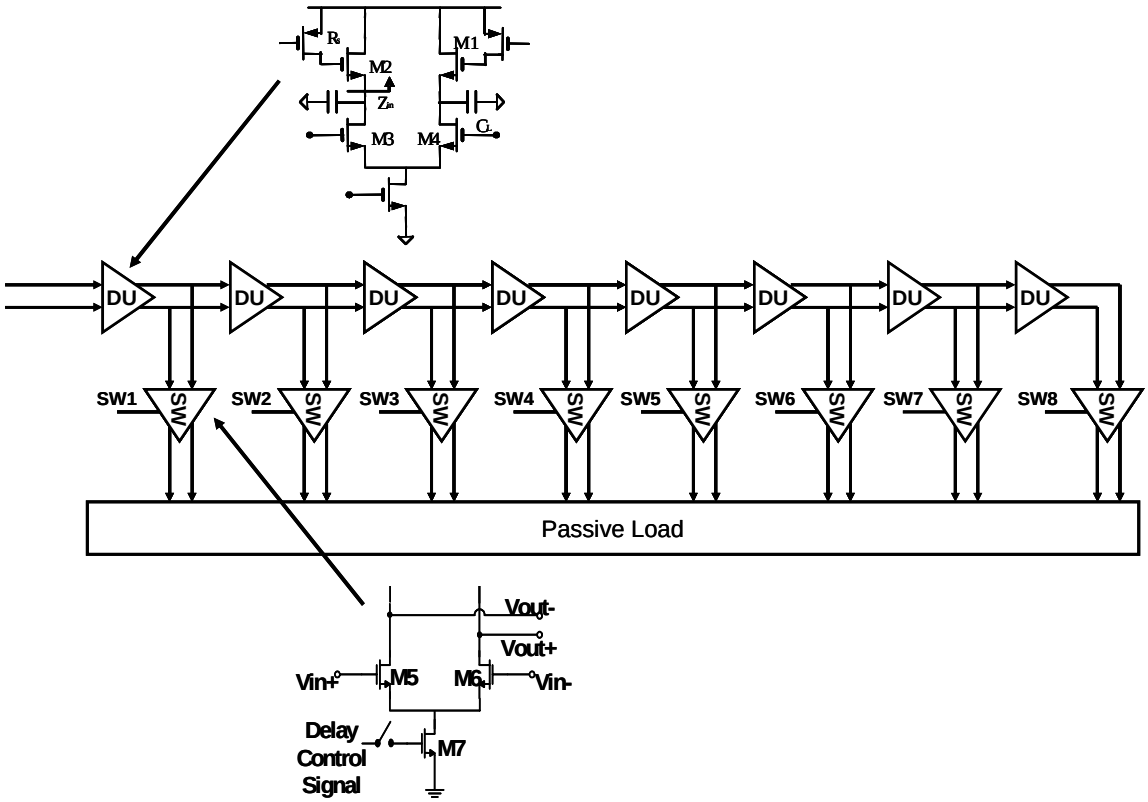


Figure 4.24. Schematic of a temporal alignment delay line.

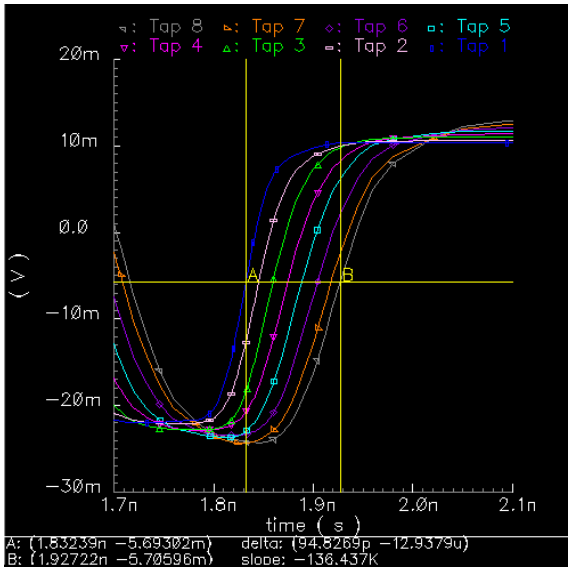


Figure 4.25. Delay simulation result of the designed temporal alignment delay line circuit.

4.4. MEASURED RESULTS

In this section, the measured basic functions of the fabricated building block circuits are presented and compared to the circuit simulation results in the previous sections. Then, system performances of the FFI IC and the NEXT noise cancellation IC are measured. The corresponding measurement results are presented and analyzed. Additionally, the measurement setup and the procedures are described in detail.

4.4.1. BACKPLANE EQUALIZATION

Firstly, the basic functions of the 4-tap FIR filter are measured. Then, the equalization performances are measured for the 10-Gbit/sec NRZ and 20-Gbit/sec 4-PAM signals over 20-in FR-4 backplane channel. Figure 4.26 shows the experiment setup for the

measurement of the FFE IC performances. The setup is consisted of a Bit-Error Rate Tester (BERT), DC sources, a Digital Sampling Oscilloscope (DSO) and FR-4 backplane PCB board with two daughter cards. The BERT generates the differential-ended transmit signal at the pre-determined data speed. This input signal is connected to the FFE IC for the basic filter functions, i.e. tap delay and gain characteristics. Then, the FFE output signal is provided to the DSO for verification of the filter functions.

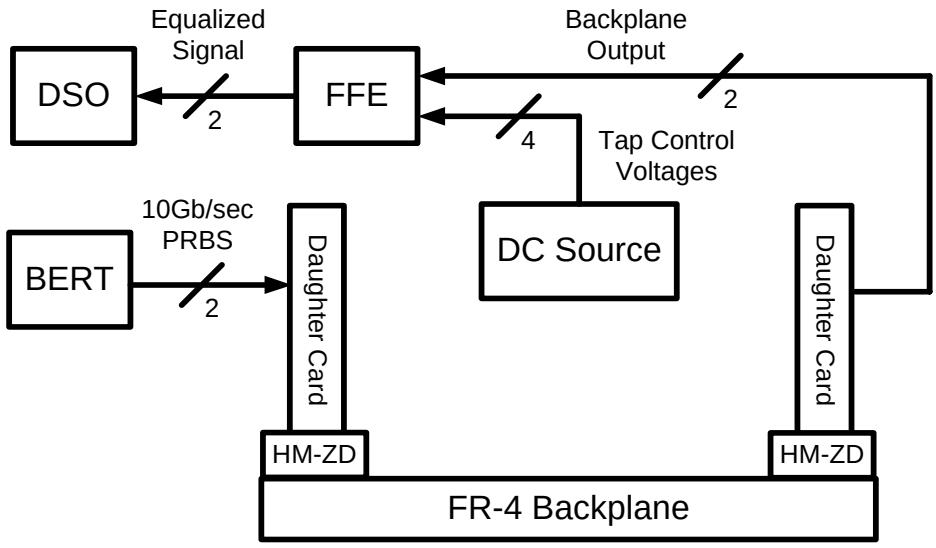


Figure 4.26. Experiment setup for measurement of the fabricated CMOS FFE IC performance.

Once the basic functionality of the 4-tap FIR filter IC is verified, then, the transmit signal is connected to the daughter card for the equalization performance measurement. The corresponding channel output signals are obtained from the daughter card at the other end of the backplane board. These channel output signals are fed into the FFE IC for the equalization. The DC sources provide the tap gain control voltages from 400 mV

~ 1.4 V for the linear gain between -1 ~ +1. Finally, equalizer output signal is connected to the DSO and the corresponding waveform and eye-diagram are observed. This FFE IC is manipulated on the probe station. Figure 4.27 shows the picture of the actual experiment setup illustrated in Figure 4.26. Table 4.1 summarizes the detailed specifications of the equipments used in this setup.

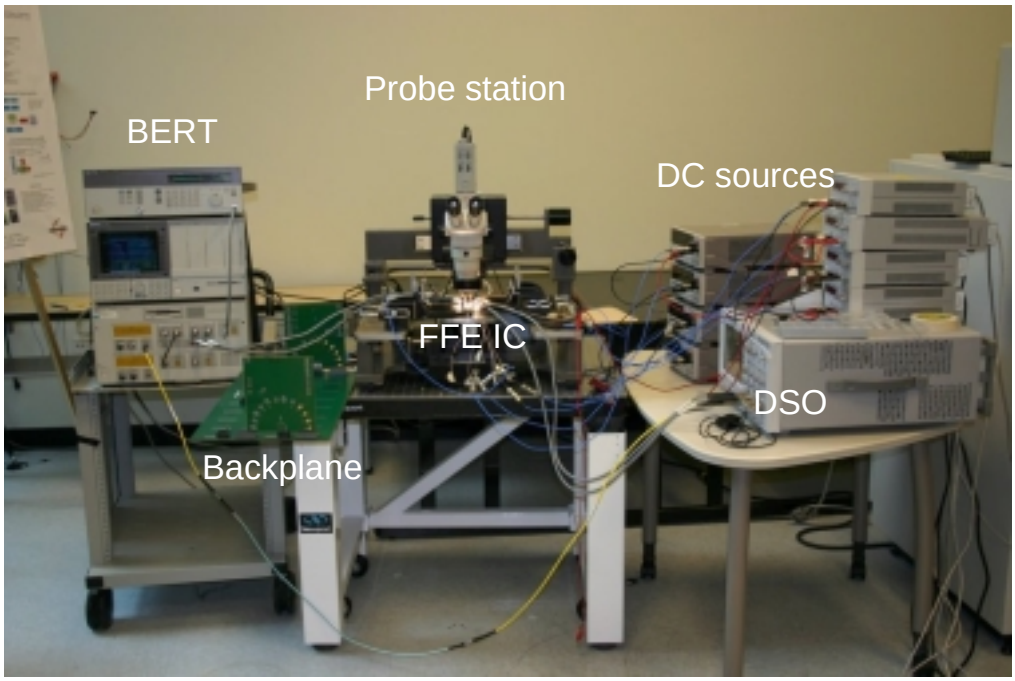


Figure 4.27. Picture of the experiment setup for the FFE IC measurement.

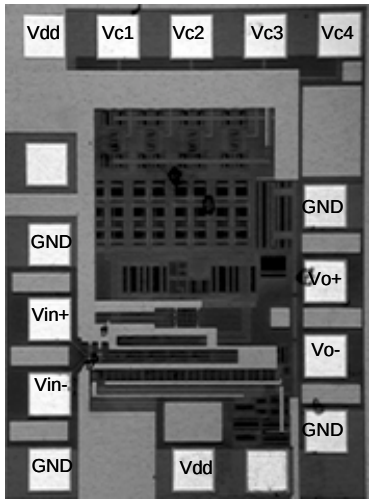


Figure 4.28. Micro-photograph of the fabricated CMOS FFE IC.

Table 4.1. Summary of the equipments used in the FFE IC measurement setup.

Item	Features	Quantities
Vector Network Analyzer	4-port differential-ended Frequency 100KHz - 40GHz	1 set
Digital Sampling Oscilloscope	4 input channels Max. sampling 40GS/sec	1 set
Bit Error Tester	10Gb/sec	1 set
Probe station		1 set
DC power supply	Dual channel Max. current 2 A	7 ea.
Cables	3.5mm SMA connector type	6 ea.
Probes	GSSG differential-ended 150um pitch	2 ea.

4.4.1.1) Tap delay line performance

Figure 4.29 shows the measured response of the delay line used in this equalizer. The 2-GHz clock signal is used as an input signal source. Each waveform is the result of the one tap coefficient being set to one while all the others are set to zero. The measurement result shows that 33-ps tap delay is achieved and is agreed with the circuit simulation as well as the system simulation result.

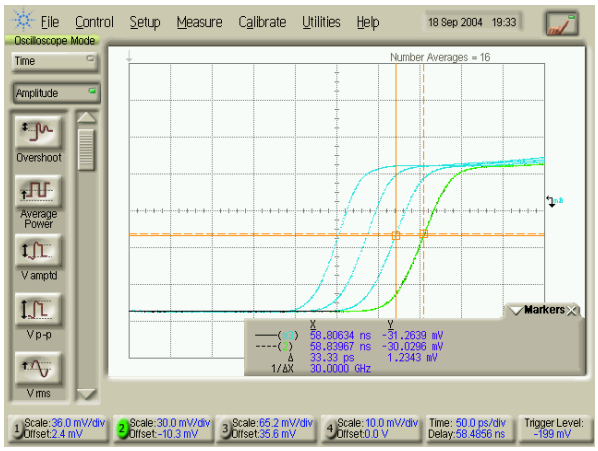


Figure 4.29. Measurement result of the 33-ps tap delay with pulse train input signal.

4.4.1.2) Multiplier cell performance

Figure 4.30 shows the proposed multiplier cell functional measurement result. A control voltage from 700 mV ~ 1.4 V is applied for gain variation. At the folded gain control block shown in Figure 4.4, Vcontrol- was fixed to 900 mV and Vcontrol+ was changed from 700 mV ~ 1.4 V to provide tap coefficient variation. For a clear view of the multiplier functionality, a 2-Gbit/sec Pseudo Random Bit Sequence (PRBS) signal as an input source.

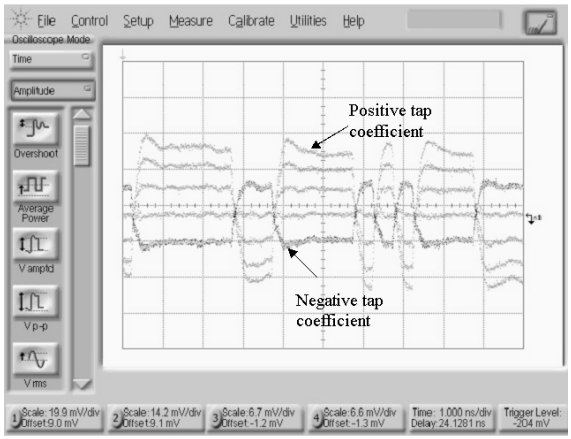
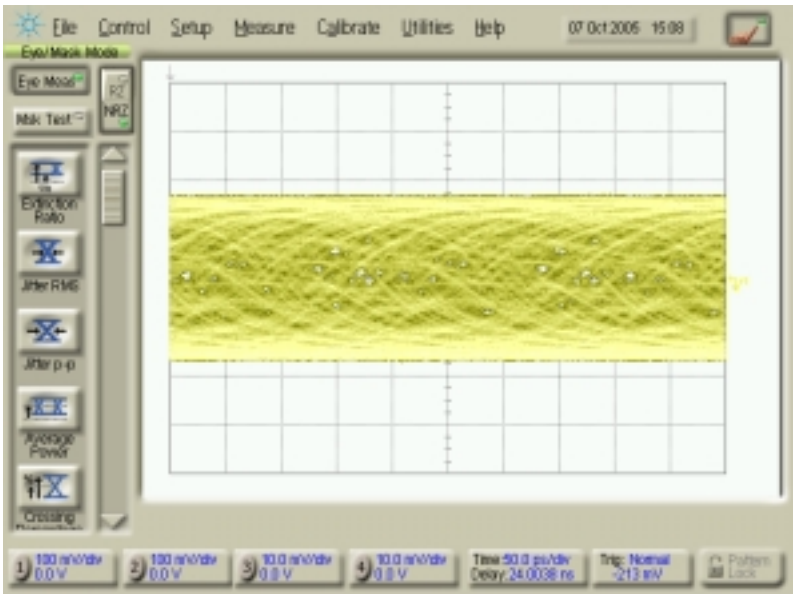


Figure 4.30. FFE output waveforms for the tap gain variation.

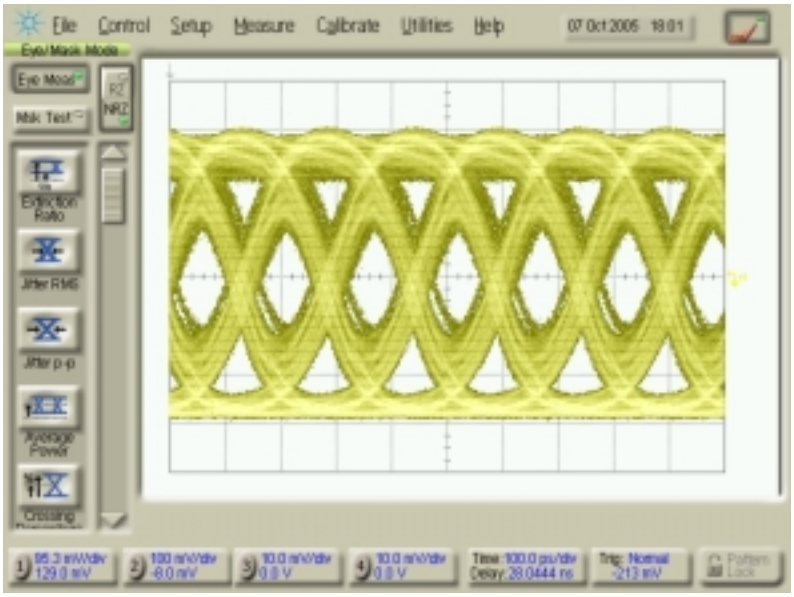
4.4.1.3) Equalization performance

Finally, Figure 4.31 and 4.32 show the equalization performances for a 10-Gbit/sec NRZ signal and a 20-Gbit/sec 4-PAM signal through the 20-inch backplane channel, respectively. The common mode voltage level at the FFE input is designed to operate at 980 mV and maintain enough voltage headroom at the passive load due to the folded gain control structure. The overall power consumption of the equalizer circuit is 7.3 mW with 1.8-V power supply voltage.

The measurement results in this section show that the implemented CMOS FFE IC successfully compensates the 20-in FR-4 legacy backplane channel loss. Consequently, the system concept of the suggested equalization technique was verified and realized using the practical IC implementation techniques.

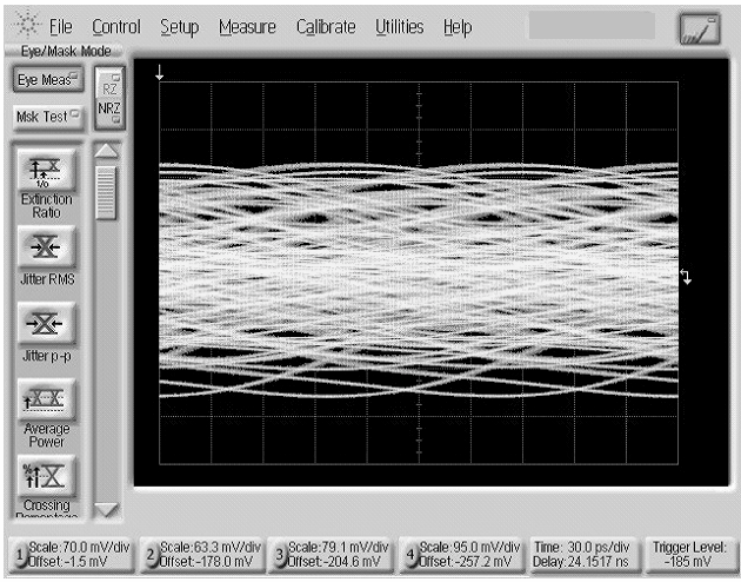


(a)

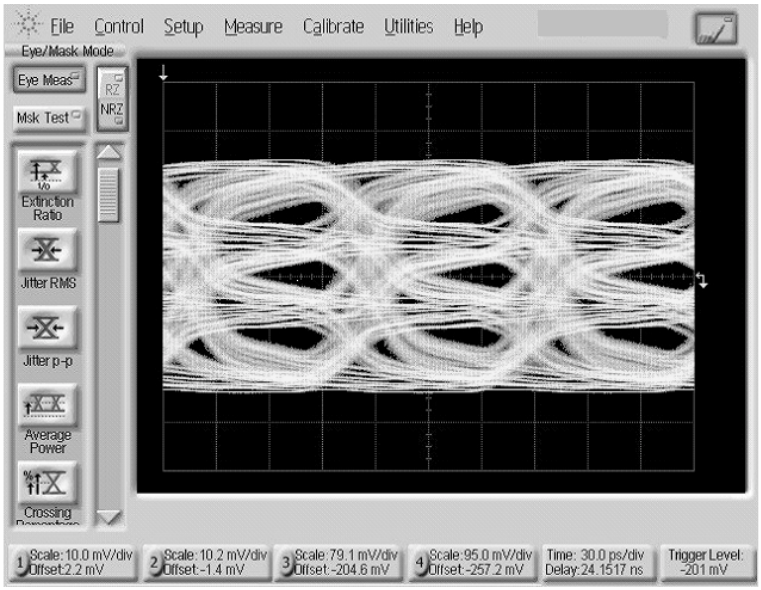


(b)

Figure 4.31. Eye diagrams of 20-in FR-4 backplane channel out for 10-Gbit/sec NRZ signal (a) before equalization and (b) after equalization.



(a)



(b)

Figure 4.32. Eye diagrams of 20-in FR-4 backplane channel out for 20-Gbit/sec 4-PAM signal (a) before equalization and (b) after equalization.

4.4.2. NEXT NOISE CANCELLATION

In this section, the building block ICs of the fabricated NEXT noise canceller are measured. Firstly, in order to verify the NEXT channel emulation performance, the active tunable PZ filter and the 7-tap FIR filter IC are characterized. Specifically, the frequency response and the step response of the PZ filter IC are adjusted to the actual NEXT channel characteristics. The 7-tap FIR filter is characterized to verify the basic function of the FIR filter. Then, channel emulation performance is characterized. Moreover, temporal alignment delay line is measured to verify the delay selectivity with 15-ps resolution. The following sections describe the measurement setups and present the measurement results of the building blocks ICs.

4.4.2.1) PZ filter performance

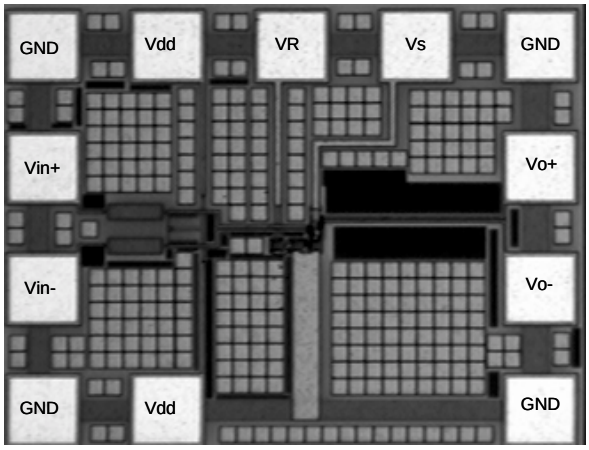


Figure 4.33. Micro-photograph of the fabricated active tunable PZ filter IC.

Figure 4.33 shows the micro-photograph of the fabricated active tunable PZ filter IC. In order to measure the frequency response of this filter, the S-parameters are

characterized with a 4-port VNA as shown in Figure 4.34. This 4-port VNA sweeps the differential-ended reference signal. These reference signals are fed into the PZ filter input pads. The DC source provides the control voltages V_R and V_S for the corner frequency tuning and gain control, respectively. The resulting output signals are compared to the reference signals in the 4-port VNA.

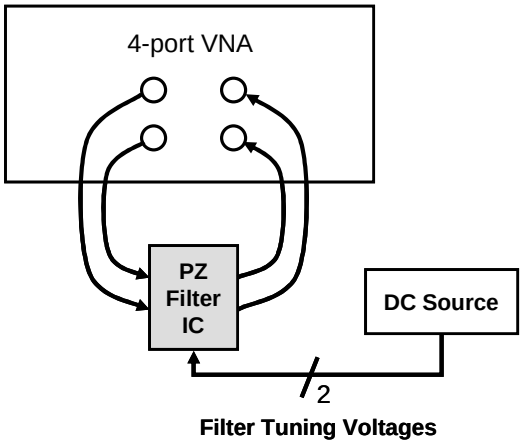
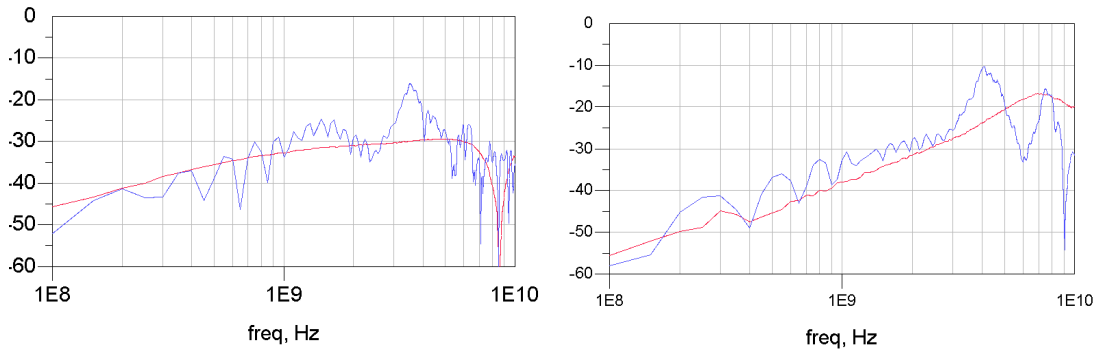


Figure 4.34. Frequency response measurement setup of the active tunable PZ filter IC.



(a) (b)

Figure 4.35. Frequency responses of the active tunable PZ filter and the actual NEXT channel for (a) the connector type A and (b) type B.

Figure 4.35 shows the measured filter frequency responses tuned to match the NEXT channel responses of the connector type A and B. The emulated channel responses are well matched to the actual NEXT channel responses.

Additionally, step responses of the PZ filter IC are measured for the different control voltage conditions to match the three connector types A, B and C. Figure 4.36 shows the step response measurement setup for the PZ filter IC. The BERT generates 1-Gbit/sec PRBS signal fed into the PZ filter. By the control voltage V_R value, the corner frequency is tuned. The resulting step responses are measured by the DSO.

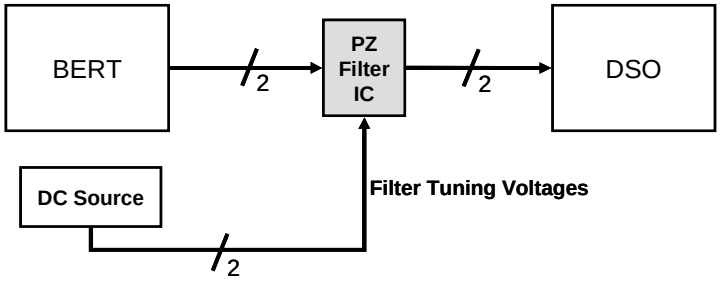


Figure 4.36. Step response measurement setup

Figure 4.37 shows the measured step responses with the control voltage conditions to match the channel characteristics of three connector types A, B and C. As the corner frequency is increases by changing the control voltage V_R, the resulting step responses has smaller DC power and the corresponding transition spikes become narrower. These step response measurement results are agreed with the system simulation results in chapter 3.

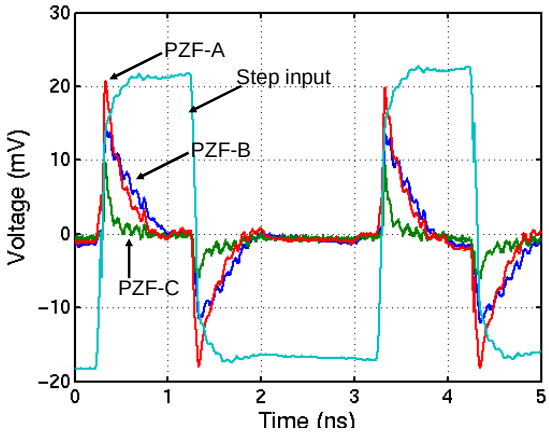


Figure 4.37. Measured step responses with the control voltage conditions to match the channel characteristics of three connector types A, B and C.

4.4.2.2) 7-tap FIR filter performance

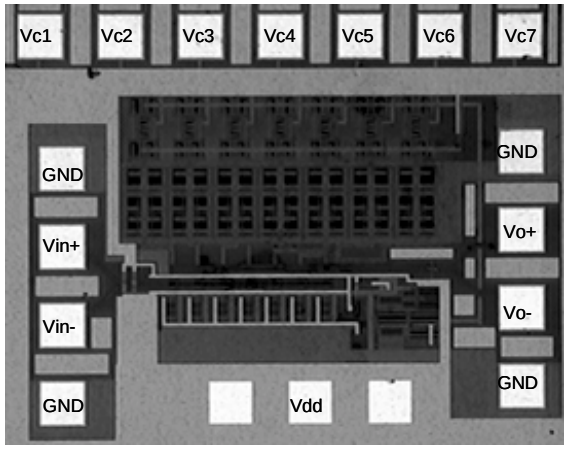
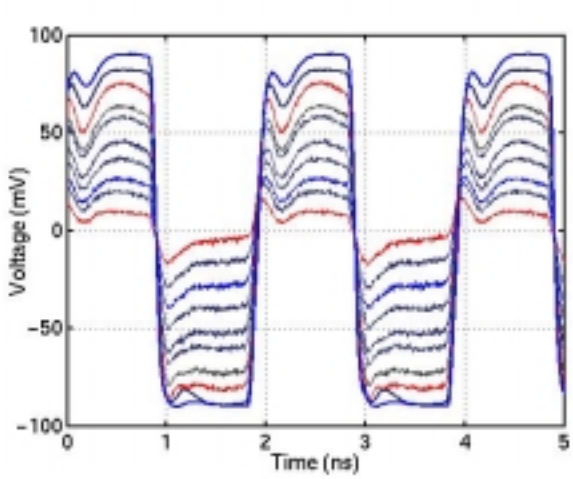


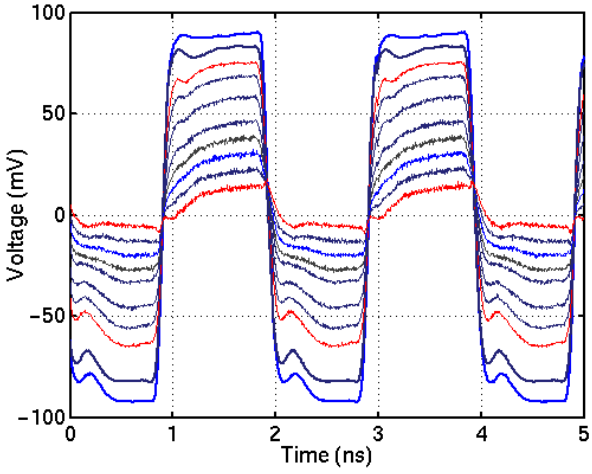
Figure 4.38. Micro-photograph of the fabricated 7-tap FIR filter IC.

Figure 4.38 shows the micro-photograph of the fabricated 7-tap FIR filter IC. In order to measure the NEXT channel emulation performance, the experiment setup, shown in Figure 4.26, is used. A 1-GHz clock signal is fed into the 7-tap FIR filter IC. The DC sources provide gain control voltages Vc1 ~ Vc7. These tap gains are set to zero by

applying the tap gain control voltage of 900 mV. Meanwhile, negative tap gain can be achieved by changing this control voltage from 400 mV ~ 900 mV, as shown in Figure 4.39 (a). Also, positive gain can be achieved by providing the control voltage of 900 mV ~ 1.4 V, as shown in Figure 4.39 (b).



(a)



(b)

Figure 4.39. 7-tap FIR filter output waveforms amplified with (a) negative tap gains and (b) positive tap gains.

The NEXT channels considered in this work have high-pass frequency responses. In order to emulate these NEXT channels, the 7-tap FIR filter must provide the high-pass filtered step response as shown in Figure 4.37. By applying the opposite-polarity tap gains to this 7-tap FIR filter IC, the high-pass filtered step response can be achieved as shown in Figure 4.40. These step responses were obtained by applying zero tap gain to every tap except for just two taps: (i) tap 1 and tap 2, (ii) tap 1 and tap 3, and (iii) tap 1 and tap 4. These two taps were set to have the maximum tap gain values with opposite polarity each other, i.e. +1 and -1. From the Figure 4.40, the width of the step response is changed by selecting the combination of two taps with opposite gains. In other words, the fabricated 7-tap FIR filter emulates the NEXT channel response with the tuning feature.

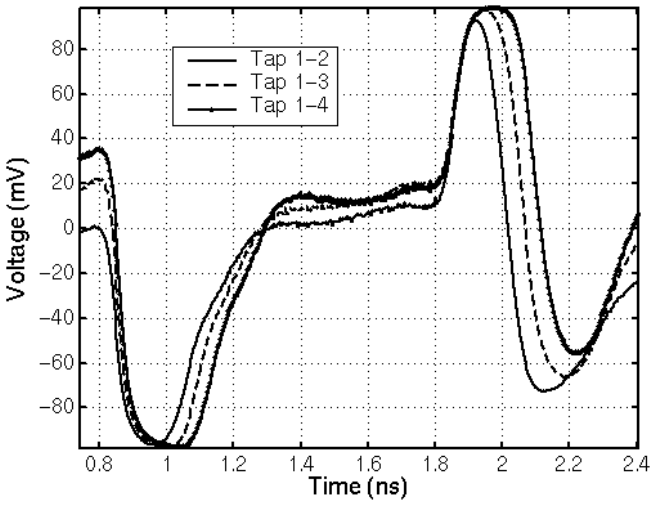


Figure 4.40. Step response measurement result of the 7-tap FIR filter IC.

4.4.2.3) Temporal alignment delay line performance

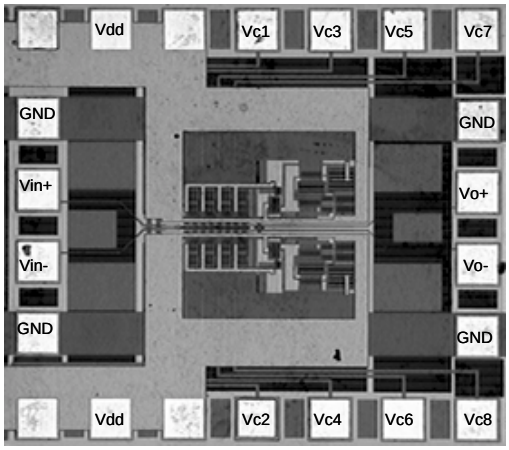


Figure 4.41. Micro-photograph of the fabricated CMOS temporal alignment delay line IC

Figure 4.41 shows the micro-photograph of the fabricated CMOS temporal alignment delay line IC. In order to characterize the delay performance, the experiment setup, shown in Figure 4.42 is used. A 2-Gbit/sec PRBS signal from the BERT is fed into the delay line IC. By manipulating the tap-selection switch control voltage Vc1 ~ Vc8, the corresponding output signal has the controlled delay value with 15-ps resolution. DC sources provide these switch control voltages of 0 V or 500 mV to turn off or to turn on the switch, respectively.

Figure 4.43 shows the measured output waveforms of the temporal alignment delay line IC. Except for just one switch for the first tap, every switch was turned off and the resulting output waveform was recorded. This procedure was repeated for the second tap through the 8th tap. The resulting measured waveforms were plotted to show the total delay of 100 ps and 15-ps delay control resolution as expected in the circuit simulation and the system simulation results.

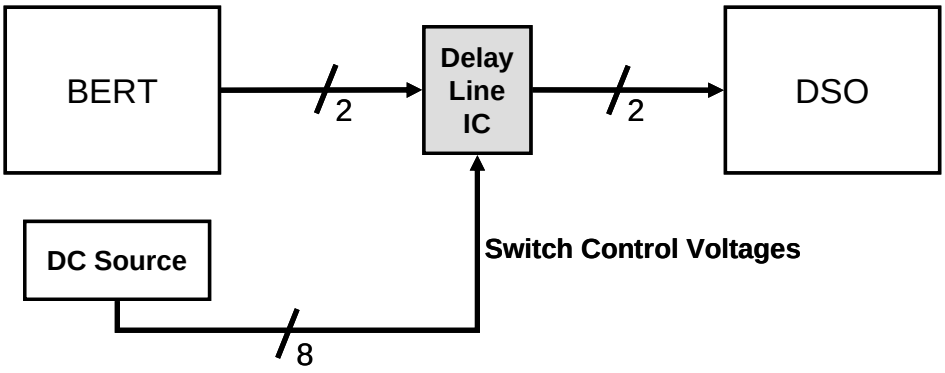


Figure 4.42. Temporal alignment delay line measurement setup.

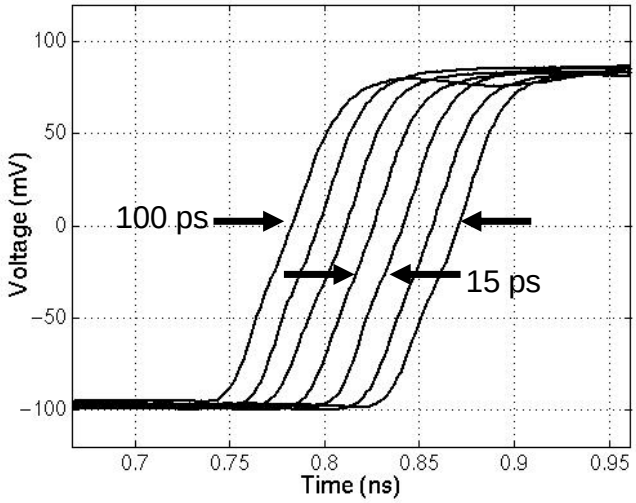


Figure 4.43. Measured output waveforms of the temporal alignment delay line IC

The measurement results provided in the section 4.4.3 showed that the implemented NEXT canceller building block ICs successfully met the performance requirements provided by the circuit and system simulations. Consequently, the system concept of the suggested NEXT noise cancellation technique was verified and realized using the practical IC implementation techniques.

CHAPTER V

SUMMARY AND FUTURE WORK

The target of this research work is to develop the solution to increase data throughput and to improve link quality in the legacy backplane application. In order to mitigate the backplane channel loss and connector coupling effects, the combined solution of the FFE and NEXT noise cancellation technique were suggested. This combined system solution was implemented with CMOS IC technology. The experiment results showed the feasibility of 20-Gbit/sec transmission over 20-in FR4 legacy backplane channel by virtue of the developed FFE and NEXT noise canceller ICs.

This dissertation showed the first 20-Gbit/sec data rate backplane equalizer based on 0.18-um CMOS technology. Moreover, the NEXT noise canceller CMOS IC adjustable to the connector types was shown firstly in this dissertation. Specifically, the active tunable PZ filter was developed for the fist time in the backplane NEXT noise cancellation application.

The original contribution of this dissertation includes:

1. First 0.18-um CMOS FFE for 20-Gbit/sec throughput over 20-in FR4 legacy backplane channel.
2. First 0.18-um CMOS NEXT noise canceller adjustable to various types of backplane connectors.
3. First investigation of a combined system solution for equalization and NEXT noise cancellation for 20-Gbit/sec backplane transmission.

4. Representation of a systematic work flow to develop system/IC solution for backplane channel effects.
5. First examination of the feasibility of 4-PAM as an alternative signaling scheme for 20-Gbit/sec transmission in legacy backplane environment.

This dissertation began with the introduction of the primary challenges of the backplane signaling environment– loss and crosstalk noise. In the chapter 2, the channel characteristics of the 20-in FR4 legacy backplane were measured with 4-port VNA to derive the corresponding behavioral channel model. The impact of the backplane channel loss on signal integrity was investigated by experiments. The experiment results showed that the NRZ signal transmission beyond 5 Gbit/sec required the equalization technique to compensate the channel loss effect. Meanwhile, the coupling channel characteristics were characterized and classified to FEXT and NEXT noise channel. The NEXT noise was turned out to be dominant over the FEXT noise for the data transmission over the legacy backplane environment. The NEXT channel characteristic has high-pass filter response and its corner frequency depends on the geometry of the connector. The corresponding NEXT channel responses of three typical backplane connectors (i.e. type A - GBX, type B - HSD, and type C - HM-ZD) have the corner frequency values of 3, 4, and 5 GHz, respectively. The NEXT noise impact on signal integrity was simulated and the result showed that the NEXT noise is another major noise component for the legacy backplane application beyond 6-Gbit/sec. From the investigation of 4-PAM as an alternative signaling scheme of the NRZ, 4-PAM signaling scheme turned out to experience less channel loss and NEXT noise effects compared to the NRZ signaling

shem. Therefore, 4-PAM was considered a candidate for 20-Gbit/sec data transmission over FR4 legacy backplane channels.

The chapter 3 provided the historical background of equalization and noise cancellation techniques. From the system simulation to investigate the optimum equalizer scheme, the receiver-side FFE with 4-tap FIR filter structure was adopted for the considered legacy backplane channel. The 4-tap FIR filter consists of tap delay line with 33-ps tap spacing and bi-polar amplifiers to provide tap coefficients calculated with the MMSE algorithm. Moreover, the system architecture was suggested for the suggested NEXT noise cancellation technique, having two stages of noise cancellation, i.e. coarse- and fine-cancellation. The system requirements of the building blocks, i.e. 7-tap FIR filter, tunable active Pole-Zero (PZ) filter, and a temporal alignment delay line were obtained from the system simulation. From the simulation result of the noise cancellation performance, the suggested NEXT noise cancellation technique achieved SNR improvement of 6 dB

In the chapter 4, the IC implementation of the suggested FFE and NEXT noise cancellation technique was discussed in detail. An 0.18-um CMOS 4-tap FIR filter IC was developed for channel loss compensation over the 20-in FR4 legacy backplane channel. An active delay line topology was adopted for the tap delay line of the FIR filter. One of the major challenging parts in the active delay line design was to satisfy the required bandwidth for 10-GHz signal operation. For the broadband circuit design, several circuit topologies were studied in this dissertation. From the literature survey, inductive peaking was chosen as the best candidate for the broadband operation. However inductive peaking technique still requires on-chip inductor, it is desirable to

replace the inductors with active components. In this dissertation, the NMOS source follower was used as load with NMOS differential pair to emulate the inductive effect on the desired frequency range, therefore it generated the peaking effect at the edge of 3 dB bandwidth. The simulation results ensured the enhanced bandwidth compared to the differential pair with passive resistive load. In order to verify the equalization performance of the fabricated FFE IC, 10-Gbit/sec NRZ and 20-Gbit/sec 4-PAM signal were experimented for the 20-in FR4 legacy backplane channel. The experiment results showed the feasibility of 20-Gbit/sec data transmission over legacy backplane environment for the first time.

The building block ICs of the suggested NEXT noise cancellation technique were implemented in 0.18-um CMOS process technology. For the adjustable feature to the NEXT channel response of three different connectors, an active tunable PZ filter IC was developed. Meanwhile, the implementation of 7-tap FIR filter and temporal alignment delay line ICs have severe loading effects due to the large number of taps connected directly to each other. In order to improve bandwidth characteristic, the circuit layout of these two building block ICs were optimized to have minimum parasitic effects. Moreover, the parasitic effects were extracted from the circuit layouts and reflected to the circuit simulation for the more accurate forecasting of the performance. Experiments were performed to verify the functionalities of the fabricated building block ICs of the NEXT noise canceller. Firstly, the active tunable PZ filter and the 7-tap FIR filter IC were characterized to show the NEXT channel emulation performance. Specifically, the frequency response and the step response of the PZ filter IC were adjusted to the actual NEXT channel characteristics. The measured PZ filter frequency responses successfully

tuned to match the NEXT channel responses of the connector type A and B. Additionally, the measured step responses were well matched to the actual NEXT channel step responses for three different connector type A, B, and C. Meanwhile, by applying the opposite-polarity tap gains to the 7-tap FIR filter IC, the high-pass filtered step responses were measured to show the adjustable channel emulation feature. These step responses were obtained by applying zero tap gain to every tap except for just two taps: (i) tap 1 and tap 2, (ii) tap 1 and tap 3, and (iii) tap 1 and tap 4. The measured width of the step response was changed by selecting the combination of two taps with opposite gains. In other words, the fabricated 7-tap FIR filter successfully emulated the NEXT channel response with the tuning feature. Finally, temporal alignment delay line was measured to verify the delay selectivity with 15-ps resolution. The resulting measured waveforms showed the total delay of 100 ps and 15-ps delay control resolution. The measurement results for the implemented 0.18-um CMOS NEXT canceller building block ICs successfully met the performance requirements provided by the circuit and system simulations.

The future undertakings related to this research are as follows. One of the most obvious research topic is to study the re-configurable equalization. Backplane channel loss characteristic depends on the channel length and the board material. Thus, the amount of channel equalization needs be adjusted to each channel configuration. Meanwhile, the backplane channel is quasi-static channel, i.e. barely changing in time. Once the channel configurations, i.e. channel length and board material, are determined, then the optimum equalizer setup needs to be adjusted to the corresponding channel loss effects. However, this equalizer setup is not necessarily able to be adaptive to the

changing of the channel loss characteristics. For a reconfigurable FFE IC implementation, wide-range tunable active delay line and very low speed DACs to provide tap-delay and tap-gain control voltages.

Moreover, real-time performance monitoring of the equalizer is another interesting topic for the realization of the re-configurable multi-Gbit/sec equalizer. In order to operate the equalizer IC in the optimum status, the monitoring the required amount of equalization should be performed in real time. However, the data throughput beyond 10-Gbit/sec needs several tens of GHz processing speed is needed to estimate the current status of equalization with the conventional approaches. Thus, the mixed signal implementation approach using an analog transition detector is very promising for realizing equalization of ever increasing data rate beyond several Gbit/sec.

The NEXT noise cancellation technique can be applied to the coupling or interference mitigation in the wireless signaling environment. As the multi-standard wireless signals are converged to a single wireless terminal and various multi-media applications are integrated to the terminal, the interference in the RF front-end or between analog signal paths becomes severe. The developed coupling noise cancellation technique can be modified to mitigate these coupling effects.

Multi-Input Multi-Output (MIMO) transmission technique has been adopted in various wireless standards requiring drastic increase of spectrum efficiency within limited channel bandwidth. This MIMO technique assumes uncorrelated channel characteristics between the MIMO channels. However, RF front-ends including antennas have coupling effects between signal paths, resulting in the impairment of the channel independency between each MIMO channel. Then, the corresponding channel capacity can not be

achieved as expected with the ideal uncorrelated MIMO channel scenario. Thus, the suggested coupling noise cancellation technique can be applied to improve the MIMO capacity with the MIMO channel correlation estimation method.

REFERENCES

[1] J. T. Stonick, G. Wei, J. L. Sonntag, and D. K. Weinlader, "An adaptive PAM-4 5-Gb/s Backplane Transceiver in 0.25-um CMOS," *IEEE J. Solid-State Circuits*, vol. 38, pp. 436-443, Mar. 2003.

[2] M. Maeng, F. Bien, Y. Hur, S. Chandramouli, H. Kim, Y. Kumar, C. Chun, E. Gebara, and J. Laskar, "A 0.18um CMOS Equalizer with an Improved Multiplier for 4-PAM/20Gbps Throughput Over 20-in FR-4 Backplane Channels," in *2004 IEEE MTT-S Int. Microwave Symp. Dig.*, June 2004.

[3] Y. Hur, M. Maeng, S. Chandramouli, F. Bien, E. Gebara, K. Lim, and J. Laskar, "4-PAM 20Gbs Transmission over 20-in FR-4 Backplane Channels : Channel Characterization and System Implementation," in *2003 IMAPS Advanced Technology Workshop on High-Speed Interconnect, EMC and Power*, Oct. 2003.

[4] D. Mijuskovic, "Backplane Communication: 5Gb/sec and Beyond," presented in *the Smart Network Developer Forum 2003*, Mar. 2003.

[5] F. Bien, A. Kim, M. Vrazel, E. Gebara, S. Bajekal, A. Ragvahan, Z. Nami, C. Lee, B. Schmukler, and J. Laskar, "A 0.18um CMOS Fully Integrated 6.25 Gbps Single Aggressor Multi-Rate Crosstalk Cancellation IC for Legacy Backplane and Interconnect Applications," in 2004 *IEEE Workshop on Signal Propagation on Interconnects*, May 2004.

[6] J.L. Zerbe, P.S. Chau, C.W. Werner, W.F. Stonecypher, H.J. Liaw, G.J. Yeh, T.P. Thrush, S.C. Best, and K.S. Donnelly, "A 2 Gb/s/pin 4-PAM Parallel Bus Interface with Crosstalk Cancellation, Equalization, and Integrating Receivers," in *IEEE Int. Solod-State Circuits Conf. Dig. Tech. Papers*, 2001, pp. 66-67.

[7] J.L. Zerbe, C.W. Werner, V. Stojanovic, F. Chen, J. Wei, G. Tsang, D. Kim, W.F. Stonecypher, A. Ho, T.P. Thrush, R.T. Kollipara, M.A. Horowitz, and K.S. Donnelly " Equalization and Clock Recovery for a 2.5-10 Gb/s 2-PAM/4-PAM Backplane Transceiver Cell," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2121-2130, Dec. 2003.

[8] H. Wu, J. Tierno, P. Pepeljugoski, J. Schaub, S. Gowda, J. Kash, A. Hajimiri, "Differential 4-tap and 7-tap Transverse Filters in SiGe for 10Gb/s Multimode Fiber Optic Equalization," in *ISSCC 2003*, San Francisco, CA, Feb. 2003

[9] J. Ortega *et al*, "Shielded Differential Connector Delivers Increased Bandwidth and Signal Integrity Performance," in the *Proceedings of the 49th Electronic Components and Technology Conference*, pp. 525-529, June 1999

[10] J. Nickel *et al*, "Optimized Interconnect Solution for High-Performance System Data Transmission," presented in *the IMAPS Technical Workshop*, Oct. 2003 in Palo Alto, CA

[11] F. Bien , et al., **"**A 0.18μm CMOS Fully Integrated 6.25Gbit/secec Single Aggressor Multi-Rate Crosstalk Cancellation IC for Legacy Backplane and Interconnect Applications**,"** in the proceeding of SPI-2004.

[12] R. Farjad-Rad, C. K-.K. Yang, M. A. Horowitz, "A 0.3-um CMOS 8-Gb/s 4-PAM Serial Link Transceiver," *IEEE J. Solid-State Circuits*, vol. 35, pp. 757 – 764, May 2000.

[13] M. J. Lee, W. J. Dally, J. W. Poulton, P. Chiang, S. E. Greenwood, " An 84-mW 4-Gb/s Clock and Data Recovery Circuit for Serial Link Applications," in Symp. On VLSI Circuits 2001, June 2001, pp. 149 – 152

[14] A.J. Kim, M. Vrazel, V.M. Hietala, E. Gebara, C. Pelardl, S. Bajekal, S.E. Ralph, and J. Laskar, "Equalization and the Evolution of Gb Communications," in 2003 *IEEE GaAs IC Symp. Dig. Tech. Papers*, pp. 193-196, Nov. 2003.

[15] M. H. Shakiba, "A 2.5 Gb/s adaptive cable equalizer," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1999, pp. 396-397

[16] R. He, N. Nazari, and S. Sutardja, "A DSP based receiver for 1000Base-T PHY," *IEEE Int. Solid- State Circuits Conf. Dig. Tech. Paper*s, pp. 308-309,Feb. 2001.

[17] T.-C. Lee and B. Razavi, "A 125-MHz CMOS mixed-signal equalizer for gigabit ethernet on copper wire," *IEEE Custom Integrated Circuits Conf.*, pp.131-134, June 2001.

[18] H. Wu, J. A. Tierno, P. Pepeljugoski, J. Schaub, S. Gowda, J. A. Kash, and A. Hajimiri, "Integrated Transversal Equalizers in High-Speed Fiber-Optic Systems," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2131-2137, December 2003

[19] J. T. Stonick, G.-Y. Wei, J. L. Sonntag, and D. K. Weinlader, "An adaptive PAM-4 5 Gb/s backplane transceiver in 0.25 um CMOS," *IEEE J. Solid-State Circuits*, pp. 436-443, March 2003.

[20] John G. Proakis, *Digital Communications*, 4th ed.

[21] R. Gitlin and S. Weinstein, "Fractionally-spaced equalization: An improved digital transversal equalizer," *Bell syst. Tech. J.*, vol. 60, no. 2, pp. 275-296, Feb. 1981

[22] B. Widrwo, "Aspects of network and system theory," in *Adaptive Filters*. New York: McGraw-Hill, 1983

[23] M. L. Honig and D. G. Messerschmitt, *Adaptive Filters*. Boston, MA: Kluwer, 1984

[24] R. Payne et al., "A 6.25 Gb/s Binary Adaptive DFE with First Post-Cursor Tap Cancellation for Serial Backplane Communications," in *IEEE Int. Solid-State Circuits Conf*. Feb. 2005

[25] T. W. Matthews and R. R. Spencer, "An integrated analog CMOS Viterbi detector for digital magnetic recording," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1294-1302, Dec. 1993

[26] J. Sonntag et al., "A high speed, low power PRML read channel device," *IEEE Trans. Magn.*, vol. 31, pp. 1103-1108, Mar. 1995

[27] M. Maeng, F. Bien, Y. Hur, S. Chandramouli, H. Kim, Y. Kumar, C. Chun, E. Gebara, J. Laskar, "A 0.18um CMOS Equalizer with a Improved Multiplier for 4-PAM/20Gbps Throughput Over 20-inch FR-4 Backplane Channels," *IEEE 2004 International Microwave Symposium*

[28] Y.S. Hur, M. Maeng, C. Chun, F. Bien, H. Kim, S. Chandramouli, E. Gebara, J. Laskar, "Equalization and Near-End Crosstalk (NEXT) Noise Cancellation for 20Gb/sec 4-PAM Backplane Serial I/O Interconnections," *IEEE trans. Microwave Theory and Tech vol. 53, pp. 246-255, Jan 2005*.

[29] R. C. Nongpiur, D. J. Shpak, and A. Antoniou, "Near-End Crosstalk Cancellation in xDSL Systems" pp.393-397

[30] T.- C. Lee and B. Razavi, "A 125- MHz mixed-signal echo canceller for gigabit ethernet on copper wire," *IEEE J. Solid-State Circuit*s, pp. 366- 373,March 2001.

[31] S. Bellini, P. Migliorati, S. olivieri, and L. Agarossi, "Channel Equalization and Crosstalk Cancellation for High Density Optical Recording," pp.513-518

[32] T. C. Lee, and B. Razavi, "A 125-Mhz CMOS Mixed-Signal Equalizer for Gigabit Ethernet on Copper Wire," *IEEE CICC 2001*

[33] F. Krummenacher and N. Joehl, "A 4-Mhz CMOS Continuous-Time Filter with On-Chip Automatic Tuning," *IEEE J. Solid-State Circuits*, vol. 23, pp. 750-758, June 1988

[34] D. Feucht, *Handbook of Analog Circuit Design*. San Diego, CA:Academic, 1990.

[35] E. M. cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifiers," *Proc. Inst. Electr. Eng*., vol. 110, pp. 375-389, Feb. 1963

[36] Y.-J. Jung, S.-W. Lee, D. Shin, W. Kim, C. Kim, and S.-I. Cho, "A Dual-Loop Delay-Locked Loop Using Multiple Voltage-Controlled Delay Lines," *IEEE J. Solid-State Circuits*, vol. 36, pp. 784-791, May 2001

[37] V. Vrodanov and M. Green, “A Differential Active Load and its Applications in CMOS Analog Circuit Designs”, *IEEE Transactions on Circuit and Systems-II: Analog and Digital Signal Processing*, vol. 44, no. 4, pp. 265-273, April 1997.